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Low-Power Soft Error Hardened Latch

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This paper presents a low-power soft-error hardened pulsed latch suitable for reliable circuit operation. The proposed circuit is aimed to tackle the particle hit effect on the internal nodes and on the external logic, simultaneously. The hardening method is based on redundant feedback loop to protect internal nodes, and transmission gate and Schmitt-trigger circuit to filter out transient resulting from combinational logic. The proposed circuit has less timing overhead and negative setup time. The HSPICE post-layout simulation in 90 nm CMOS technology reveals that circuit is able to recover from almost any single particle strike on internal nodes and tolerates input transients up to 130 ps of duration.

Keywords: Alpha Particles, Atmospheric Neutrons, Design for Reliability, Design for Soft Error Mitigation, Fault Tolerant Design, Single-Event Transients, Single-Event Upsets, Soft Errors, Static Latch, Hardened Latch, Reliability.

1. INTRODUCTION

In the nanometer technologies, a circuit is increasingly facing reliability issues, the most serious among them being radiation effects and resulting soft errors. Unlike the hard error which is due to permanent physical damage, soft error is a stored data change due to particle hit. The soft errors which were traditionally regarded as a reliability issue for space applications are becoming a terrestrial issue.[1–4]

In continuous advances of microelectronic technologies, due to aggressive shrinkage of device dimensions, node capacitance and power supply voltage reduction,[20] the amount of stored charge on each circuit node is becoming smaller. The smaller stored charge and higher operating frequency now make circuits more vulnerable to soft errors. This reliability issue is due to charge deposit induced directly by alpha particles or indirectly by atmospheric neutrons.[1] Alpha particle is produced by radioactive isotopes found in packaging and die materials, while atmospheric neutron is created by the interaction of cosmic ray with the earth atmosphere.[1, 3, 4]

A study on radiation flux noted that particles with lower energy level occur far more frequently than particles with higher energy level.[1] So as CMOS device size shrinks, it becomes more possible to be affected by lower energy particles, potentially leading to higher soft error rate.

Although package and process engineering may reduce alpha particle and thermal neutron problem by removing some materials from the process, but there is no physical obstacle to cosmic neutrons.[1, 4] To face this challenge, improved circuit design schemes to mitigate soft error vulnerability are becoming mainstream approach for high reliability systems.[3]

Among different building block of a digital circuit, clocked storage elements (CSEs), i.e., latches and flip-flops, are becoming more susceptible to particle strike on both external logic and its own internal nodes.[5, 10] Most common protective methods at circuit level are based on redundancy, namely temporal and spatial redundancy. The spatial redundancy based methods,[5, 10] as well as soft error resilient scan latch,[21] and even transient detection of RAZOR flip-flops[19] cannot tolerate soft error due to particle hit in combinational logic. On the other hand the temporal redundancy based latches[10] and those based on Schmitt-trigger[14] and transmission gate[18] may reduce the transient effects but has extended setup time problem and cannot protect internal nodes. The contribution of this work is to simultaneously reduce single particle hit effect on internal nodes and reduce input transient susceptibility in a latch design with less timing overhead.

The rest of this paper is organized as follows. In Section 2, starting with some basic definitions most recent

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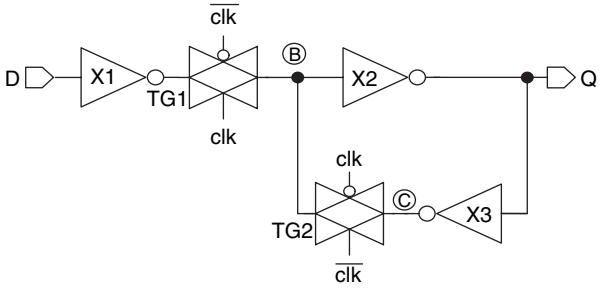

Fig. 1. Level sensitive latch.

publication and latch hardening methods will be reviewed. Section 3 proposes the soft-error hardened latch. Section 4 gives simulation results and Section 5 concludes the paper.

2. SOFT-ERROR AND LATCH-HARDENING METHODS

This section gives a brief overview of the physics of the particle hit, and reviews some recent latch hardening methods. When an energetic particle hits the drain of an off MOS transistor, it loses energy traveling in the silicon and creates free charge carries (electron and holes) in the path. The amount of charge depends on particle type (alpha or neutron), its energy, and the base silicon property. The electric field of the drain junction can collect those carries before recombining, resulting in a transient current pulse at the drain connected node.[1–4]

Generally speaking, an energized particle may hit logic gates, storage elements, or clock distribution network (CDN) of a digital circuit. In the case of logic gates, the injected current pulse causes a glitch on the output voltage of the gate, called single event transient (SET).[1,2] The shape and the duration of the SET depend on both the characteristics of the current pulse and the electrical property of the node, such as the load and driving strength of the connected gates.

When a particle directly hits an internal node of a CSE, i.e., latch or flip-flop, a sufficiently injected charge may change the stored data, resulting in a single event upset (SEU). As a second source for soft error in a CSE, a SET might be generated and propagated through the combinational logic and captured by a CSE which turn into an SEU.[3]

If a particle hits a control signal, such as the clock signal, it could generates a false control signal which results in an unwanted data latch or timing violation.[6] The rate at which soft errors occur is referred to as soft error rate (SER).

During the process of transient voltage propagation in a logic circuit, a SET could be masked by logical, electrical, or latching window masking effects.[3,8,15,25] The SET propagation is conditioned by the state of the logic since a controlling value on one input of a gate will block the propagation of an SET from another input to the output. Thus, due to logical masking a transient pulse can be propagated only through an activated path. The pulse propagation is also conditioned by the electrical masking and the pulse duration. If the pulse duration is lower than the logic transition time of a gate, it cannot be propagated through it. But if this duration exceeds the transition time of a gate,

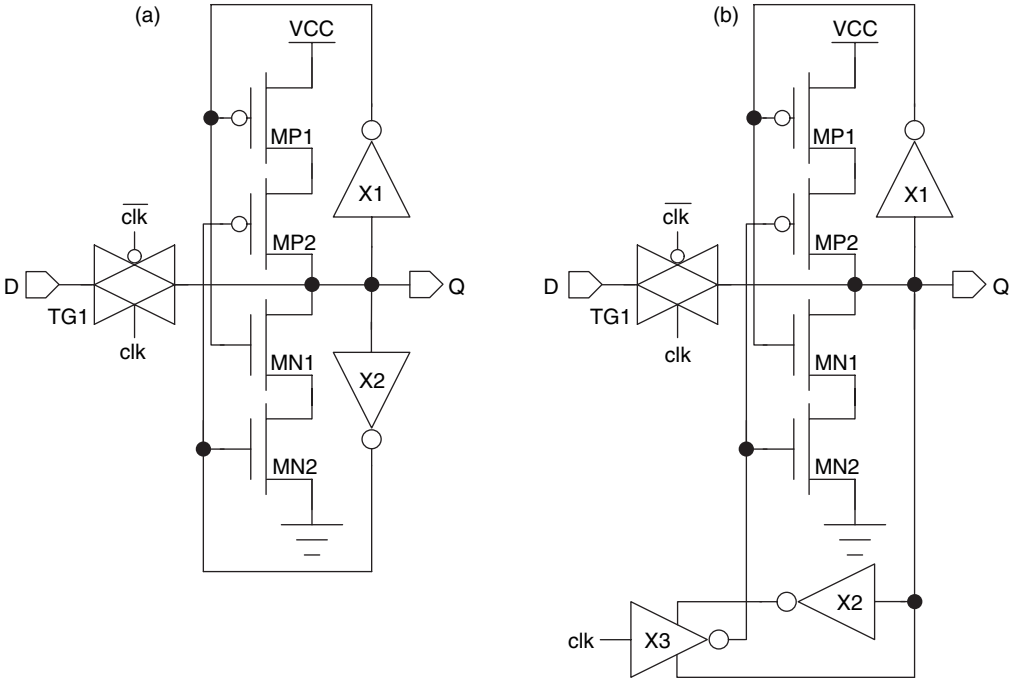

Fig. 2. Redundant feedback loop latches[3] (a) SIN-LC, (b) SIN-HR.

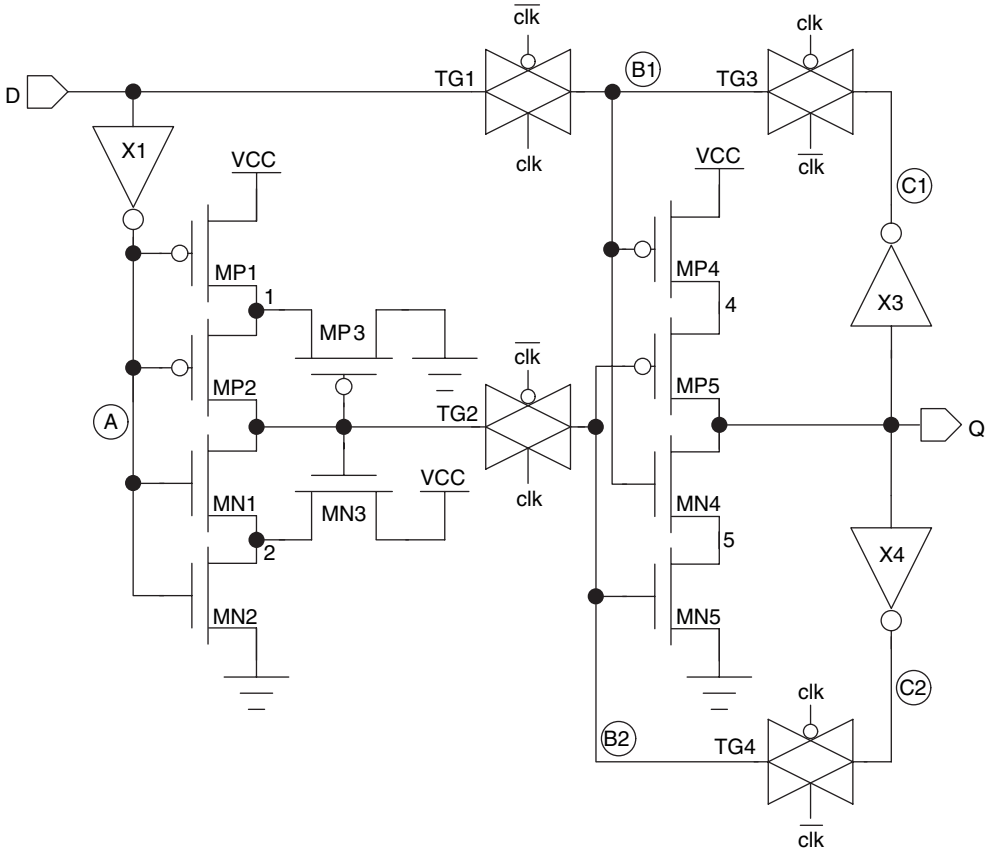

Fig. 3. The proposed dual edge-triggered soft error hardened pulsed latch (DET-SEHPL).

the pulse would be propagated without attenuation. As the last condition, when the SET reaches a CSE, it will be captured only if it reaches the CSE at the sampling window unless it will be masked.[3, 15]

Those three masking mechanisms may prevent some SETs from being latched and alleviate the soft error rate in digital systems. However, due to continuous scaling trends, increased frequency and wide spectrum of particle energy, the probability that transient voltage reaches storage elements on time and gets latched is increasing, and so does the soft error rate.[1–4]

Among different building block of a digital circuit, memories are traditionally protected by Error Correction Codes (ECC).[3] The CSEs have also received more attention recently to make them more robust to soft errors.[5, 10, 14, 24] However, recent studies indicate that logic also will be more vulnerable to soft error.[1, 3, 8, 13] Due to the fact that soft error in CSEs has two different sources, both internal design of the CSE and external connected logic needs to be considered for protection and hardening.

Node engineering,[11] gate sizing,[20] guard ring effect,[23] as well as negative feedback effect[22] are studied extensively to mitigate SET effect at logic level. The objectives of

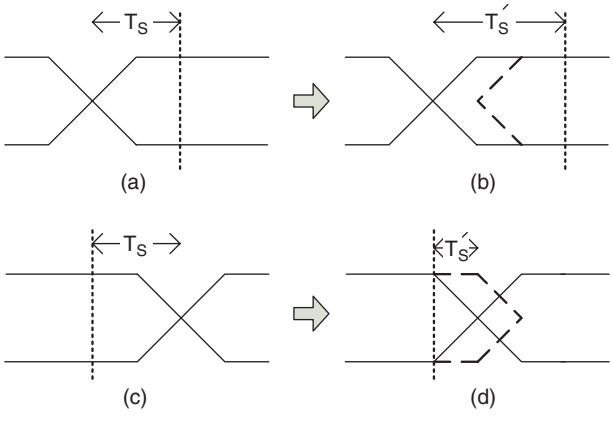

Fig. 4. Setup time variation in: (a) ordinary clocking, (b) ordinary clocking after hardening, (c) pulsed latch, and (d) pulsed clocking after applying hardening methods.

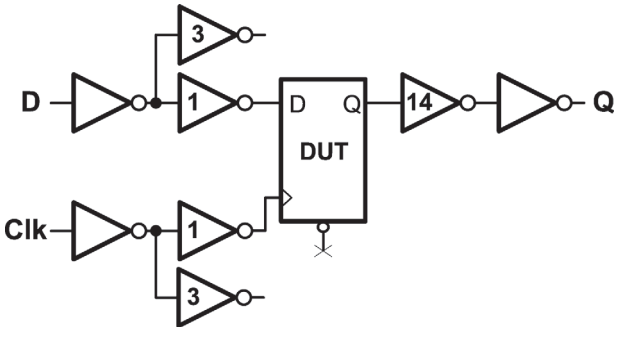

Fig. 5. Simulation Setup.[26]

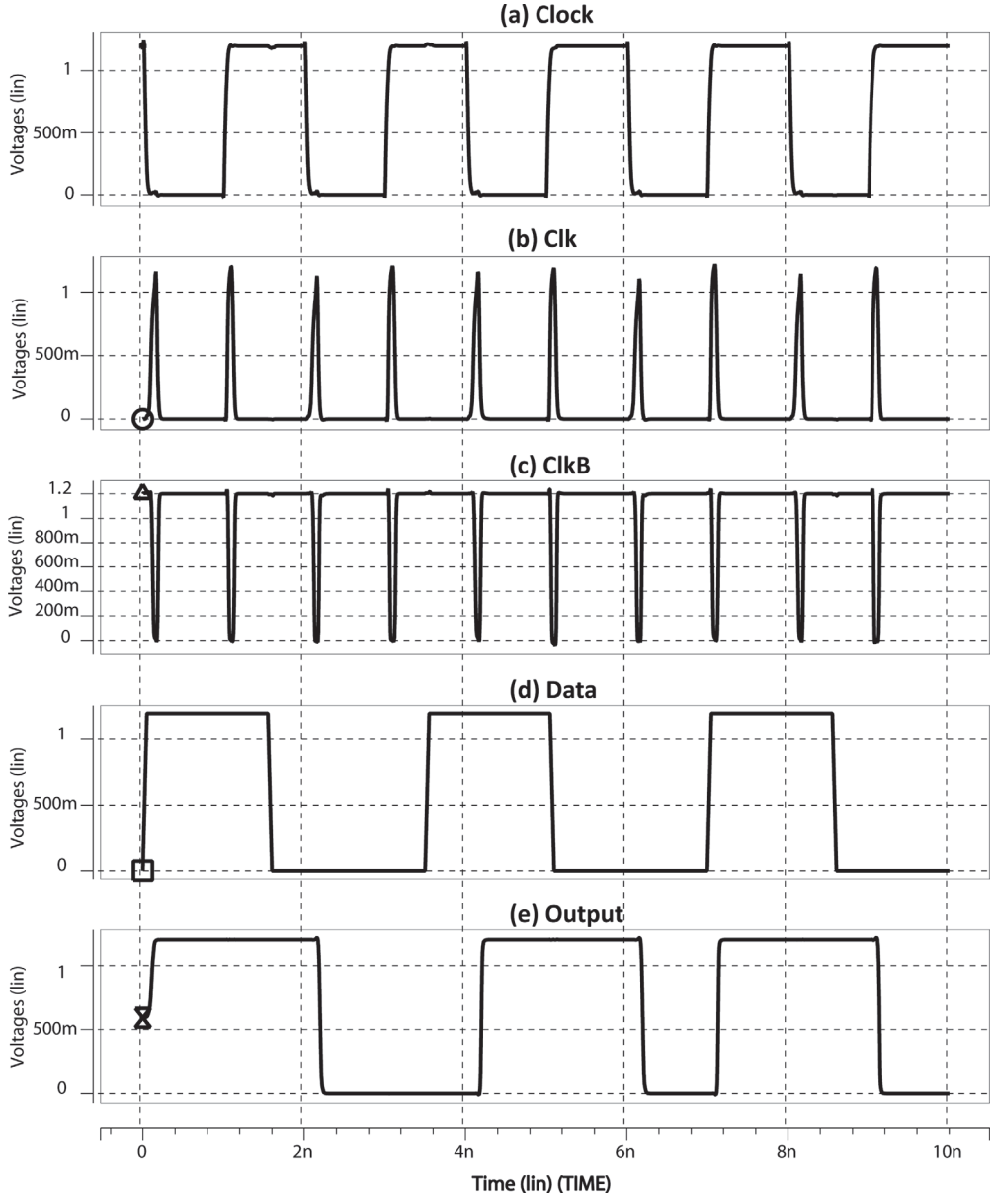

Fig. 6. Simulation result of the DET-SEHPL in normal mode operation, (a) System Clock, (b) "CLK" and (c) "CLKB" pulse generator outputs, (d) Data Input "D," and (e) latch output "Q."

those studies are to design and size logic gates of a circuit in a way that they attenuate transient pulses caused by particle strike.

The simplest form of hardening technique for latches and flip-flops is to increase stored node charge by adding resistance or capacitance,[11] but it degrade circuit speed and increase power consumption. While error-correcting and latch-hardening designs could be used to reduce the effect of SEUs, complete protection against SETs is much more difficult and involves either spatial or temporal redundancy. The spatial redundancy uses multiple copies of a given circuit with majority voting mechanism to determine correct outputs. One effective way to overcome SEU effects is to triplicate each latch of the system and use Triple Module Redundancy (TMR-latch). Although TMR-latches are highly reliable and widely used,[9] but this technique suffers from high area and energy consumption overhead.

The temporal redundancy technique uses delayed sample of the data,[10, 25] and is more acceptable for conventional designs due to its lower power consumption and area overhead. This technique can eliminate all SET pulses which have smaller duration than a certain threshold value. The major drawback of this method is its delay penalty, and the fact that it cannot guarantee fault-free operation.

The dual interlock storage element (DICE) is another soft-error hardened topology based on spatial redundancy. It has been introduced[12] and applied to a standard 6 T

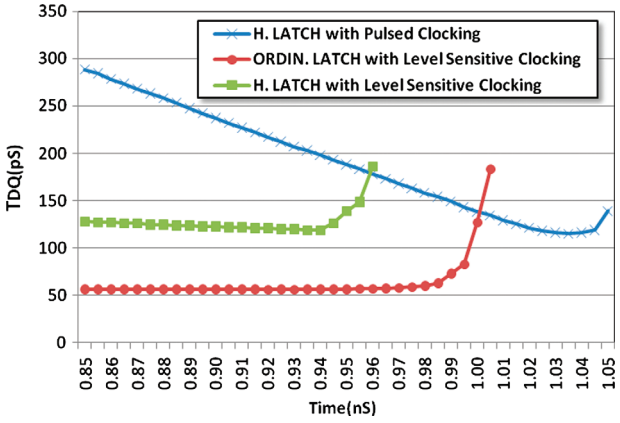

Fig. 7. Data to output delay and setup time variation of hardened latch in pulsed clocking mode (blue), ordinary latch (red) and hardened latch (green) both in level sensitive clocking.

memory cell[13] and used in a pulsed latch design of a high performance processor.[24] The hardened structure of the DICE has the potential to improve SEU robustness of the latch circuits without degrading its speed too much; however it comes up with area and power penalty,[24] and it cannot tolerate SETs.

Redundant feedback loop is a soft error hardening method applied to a basic latch. According to analyses in Ref. [5], soft error of the internal nodes in feedback loop, i.e., node B and C in Figure 1, has the major contribution to the total SER. If a particle strike causes an unexpected voltage drop or rise inside the loop during the holding mode, the stored value in the latch may change depending on the amount of deposited charge.[4, 5] Also our simulations indicate that node B in this circuit is much more sensitive than node C.

SIN-LC and SIN-HR latches[5] are proposed based on the redundant feedback loop to solve the SER issue of the basic latch. Figure 2(a) shows the detailed schematic of the SIN-LC latch. It consists of duplicating feedback loop and using C-element to make the latch output change only when both feedback loops have the same logic value. Besides sizing issue, the SIN-LC suffers from contention current drawback that occurs when the latch is in the transparent mode. The SIN-HR[5] of Figure 2(b) is proposed to solve those problems, but the main problem still exists. The FERST[10] is another latch which is also based on duplicated feedback loop idea and tries to solve the contention current problem, but it comes up with large area, timing, and power overhead.

Along with redundancy based methods, transient filtering effect of the Schmitt-trigger circuit is studied and a hardened latch based on its property is proposed.[14] The filtering effect of the transmission gate,[18] the negative feedback on SET propagation,[22] and charge absorption efficiency of the guard-ring and circuit layout effect on soft error,[23] are reported separately.

The first group of aforementioned methods[14, 18, 22, 23] deals with the external logic and the SETs. The second group,[5, 10, 12, 13, 24] as well as scan based soft error resilient latch,[21] even transient detection mechanism of RAZOR-II,[19] and DTDB[27] flip-flops, deals with internal nodes and tries to mitigate the SEU susceptibility but cannot tolerate soft error due to capturing SETs. Thus, circuit level hardening techniques are required which can tolerate SET and SEU simultaneously.

3. PROPOSED SOFT ERROR HARDENED LATCH

This section proposes a dual edge-triggered soft error hardened pulsed latch (DET-SEHPL) which is based on the temporal redundancy, dual feedback loop, and incorporates extra glitch filtering to tolerate SET and SEU simultaneously. The detailed schematic of proposed latch is shown in Figure 3.

Data redundancy and glitch filtering is used to reduce SET coming from combinational logic. The glitch filtering is done in two steps. First, the transmission gate based filter and the Schmitt-trigger circuit with hysteresis effect attenuates SETs and also adds delay to create temporal redundancy. At the second step, a C-element is used to filter out more SETs and reduce SEUs.

The proposed circuit is a pulsed latch and using a general purpose pulse generator, operates in transparent and hold modes as follows. The pulse generator circuit generates small duration pulses on each clock edges. During the small period of the pulses feedback loops composed by X3-TG3 and X4-TG4 pairs are open and the latch is transparent. In this circuit the data path is divided into two paths, normal and filtered. The pass transistors in the data paths, i.e., TG1 and TG2, are conducting and working as a low-pass filter.[18] The hysteresis effect in the filtered path is achieved using MP3 and MN3. During transparent time, input data and its delayed/filtered version are applied to the C-element composed by MP4, MP5, MN4, and MN5. Based on C-element property the output will change accordingly if both versions are the same, unless the previous value is preserved. In other words, the value on the data line will be latched on the condition that it is not a glitch or a transient event.

After small period of transparent pulse, the latch switches to hold state. In this period data paths are blocked and feedback loops are closed. The sensitive nodes in the proposed circuit are B1, C1, B2, and C2. If a particle hits one of those nodes, it would generate a voltage spikes but provided that it is a single particle hit and one feedback loop is affected, the dual feedback loop connection and the C-element will remove its effect.

As mentioned, temporal redundancy is used in the proposed latch to mitigate SET effects and it is implemented by adding a delay to the one of data paths. The required

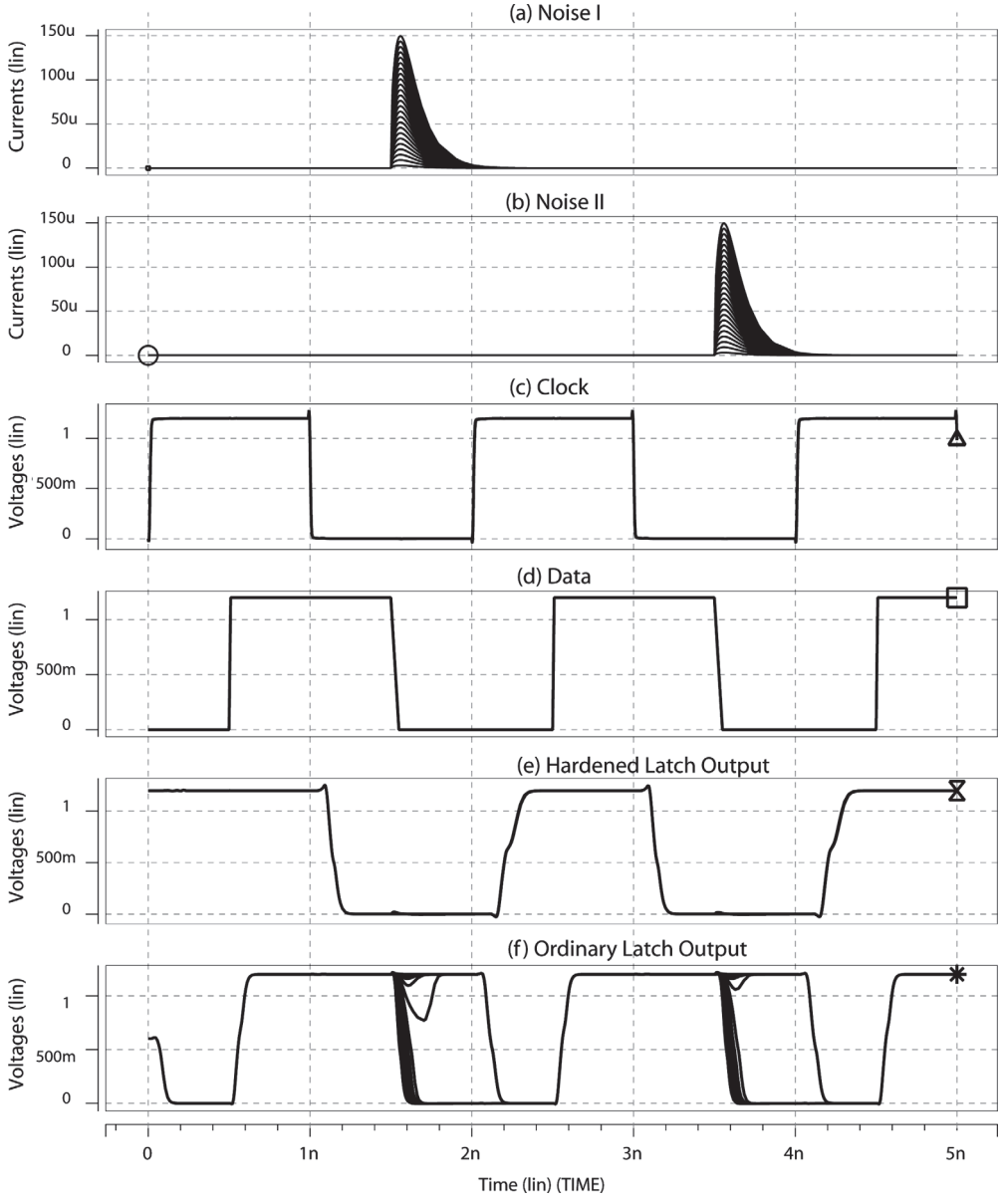

Fig. 8. Comparison of the ordinary and proposed latch operation under particle affected mode, (a) injected charge at 1.5 ns, (b) injected charge at 3.5 ns, (c) input clock, (d) input data, and (e) hardened latch output, and (f) ordinary latch output.

delay value in the data path must be longer than the duration of the possible longest SET in order to effectively filter it out. The timing diagram in Figure 4 shows the idea used in this design to reduce SET effect with less timing penalty. The timing diagram of Figure 4(a) shows the positive setup time of an ordinary latch. Applying temporal redundancy to the ordinary latch increases the setup time (Fig. 4(b)) resulting in performance penalty. As a result, window of vulnerability (WOV)[1, 3, 5, 16] to particle hit also increases. The WOV is a period in which particle hit could cause soft error.[16]

In the pulsed latches due to the soft edge property, setup time usually has a negative value (Fig. 4(c)).[17] The proposed topology uses the soft edge property and resulted negative setup time of pulsed latches to mitigate the extended setup time penalty. Applying the temporal redundancy to the pulsed latch (Fig. 4(c)) adds a positive delay value to the negative setup time, thus the setup time of hardened pulsed latch in Figure 4(d) is still smaller than the setup time of the ordinary latch.

4. EXPERIMENTAL RESULTS

The proposed latch has been implemented using 90 nm CMOS technology with 1.2 V power supply voltage. In order to have realistic input waveforms and rise/fall times, the simulation setup of Figure 5 is used for all cases.[17, 26] Due to the inverted polarity of the output in the proposed

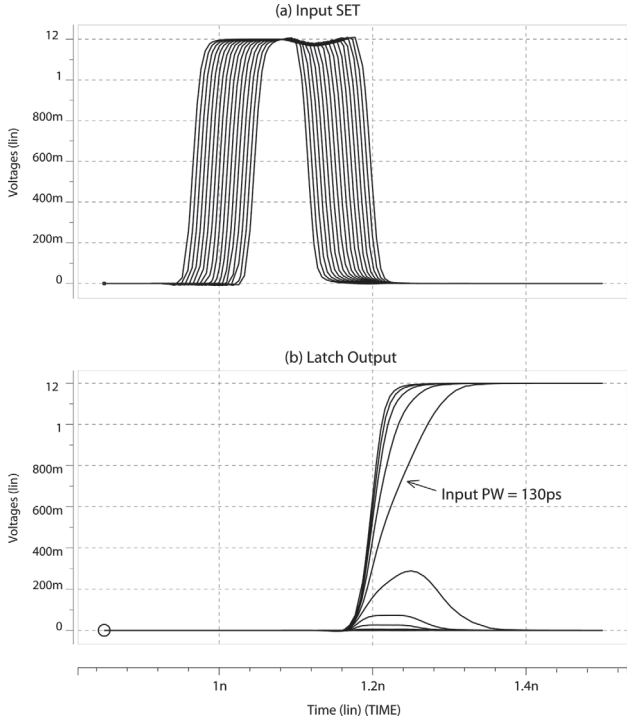

Fig. 9. SET robustness of proposed circuit, (a) input data, (b) latch output.

circuit, inverter is added to the inputs whenever that it was needed.

The performance of the proposed latch has been verified in the two normal and particle affected modes. The particle affected mode simulation is also divided in two modes. The first particle affected mode simulations is the SEU verification, which verifies robustness of the circuit against the particles which hit on the internal sensitive nodes. The second particle affected mode simulations is the SET robustness, which verifies filtering effect and circuit tolerance against particle hit on combinational part and the resulted SET, which may reaches the latch on the sampling window.

The normal mode operation result of the proposed circuit is shown in Figures 6 and 7 indicates its basic timing parameters such as the data to output delay (T_{DQ}) and setup time variation respect to the data arrival (T_{DC}) time. This figure also gives the setup time and delay variation for the ordinary latch of Figure 1 and the proposed circuit, both in level sensitive clocking for comparison. The flat region on the data-to-output delay and negative setup time of proposed hardened latch reveals that if data arrives close to the clock edge or even 40 ps after clock edge, the latch is still able to capture it correctly.[17] While the same circuit in level sensitive clocking mode and with almost same output delay, comes with large positive setup time. The remaining extra negative setup time could be invested in the input path by adding extra delay to filter out more SETs.

Table I. Different latches' setup time, delay, power consumption and power-delay-product comparison (*TMR specification is estimated).

Latch type	Setup time (ps)	Delay (ps)	Power (μW)	PDP (fJ)
Basic latch (Fig. 1)	20	55	8.0	0.44
Figure 3 in level sensitive	60	120	23.3	2.8
Figure 3 in pulsed mode	−35	120	21.2	2.5
TMR Latch*	60	120	24	2.88

As mentioned in the Section 2, regardless of the particle type (alpha particle or neutron), when it hits the drain of a MOSFET and loses energy, electron–hole pairs are generated and the resulting charges can be rapidly collected by the high electric field of the drain which create a transient current pulse at that node.[1, 3, 4] The whole process of particle hit, charge deposit, and its distribution is complicated. But for the sake of simplicity, it is modeled by exponential current sources with varying current levels and time constants to emulate different particles and varying energy levels.[1, 5, 10]

The SEU robustness of the proposed circuit is verified by charge injection at 1.5 ns and 2.5 ns to the nodes B1 and C1 in Figure 3, and the same current level injection is done to nodes B and C of the ordinary latch in Figure 1, for robustness comparison. Figure 7 shows the simulation results and indicates that the ordinary latch output is unstable after 12.6 fC and 19.8 fC charge injection to nodes B and C, respectively. While the dual feedback structure of the proposed circuit is able to recover from almost any single particle hit and resulting charge deposit.

The particle hit on combinational logic causes voltage glitch at the affected gate's output. After passing levels of logics, those glitches convert to voltage pulses which may reaches to the latch "on-time" and gets captured.[1, 3] For the SET robustness verifications, this phenomenon is modeled by voltage pulses with different width on the data line which each has proper arrival time according to setup and hold times, to represent various particles with different energy levels. Figure 9 shows the simulation results and indicates that the proposed latch is able to filter out SETs with up to 130 ps pulse width. Table I compares the timing and power specifications of the basic latch and the proposed circuit with the TMR latch as a representative of hardened latches.

5. CONCLUSION

In this work, an SER-Hardened pulsed latch is proposed. The proposed latch was able to tolerate particle strike and resulted SEU on internal nodes, as well as SET occurring in combinational logic. The HSPICE simulation on 90 nm CMOS technology is conducted to precisely evaluate the proposed circuit in normal and under particle strike mode. The circuit operating as edge triggered CSE, was resilient to SET from combinational logic as well as SEU resulting from internal nodes. Extra reliability enhancement is achievable by careful layout design. In comparison

with the TMR-Latch as a representative for SER-hardened designs, proposed circuit had less power consumption and lower timing overhead, which make it suitable for low-power reliable applications.

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