LOW VOLTAGE BICMOS TSPC LATCH FOR HIGH PERFORMANCE DIGITAL SYSTEMS

*Borivoje Nikolic and Vojin G. Oklobdzija**

Department of Electrical and Computer Engineering, University of California, Davis, CA 95616, USA
*Integration, Berkeley CA 94709, USA

ABSTRACT

New true single-phase clock (TSPC) BiCMOS circuits are described. The TSPC latches are intended for use in high-performance deeply pipelined digital electronic systems. The circuits described are based on quasi-complementary BiCMOS circuit using single-phase clock. They are verified to have full-swing operation with supply voltages as low as 1.5V. The speed and power performance of the new latch is superior to previously published results, which was confirmed by simulation in 0.5μm technology.

1. INTRODUCTION

BiCMOS digital circuits are often used in digital systems where high performance is of great importance. The overall speed of those systems is enhanced by deep pipelining and the use of relatively small number of logic stages. Fig. 1 shows the diagram of single-phase clocked pipelined system, consisting of two logic blocks separated by N and P type latches. N type latches are transparent when $\phi = 1$, and opaque when $\phi = 0$, while P type latches are transparent when $\phi = 0$, and opaque when $\phi = 1$ [1]. Since the pipeline design is based on latches [2, 3], they play the key role in overall system performance. If the latch is followed by a small number of logic stages, a high fan-out is often created, placing a demand for high driving capabilities of the latch. In case of very high performance systems, the logic between the latch stages is dynamic. In this work, we propose a new latch and dynamic logic circuits implemented in BiCMOS technology, which improve the circuit performance in terms of speed as well as power. The stages are based on quasi-complementary (QC) BiCMOS inverter [4], and are suitable for low supply voltage operation. The latch is designed for use in true single phase clocked (TSPC) systems, as opposed to the master-slave latch proposed in [5], which uses two phase clock. The other advantage of the proposed latch is the possibility of incorporating logic function into the latch [3]. The parameters of the new latch were compared to previously published results [3, 7], in terms of speed, power and dependence on supply voltage.

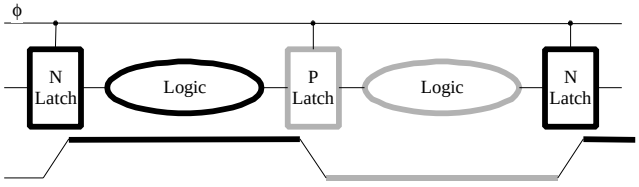

Figure 1. Single-phase pipeline

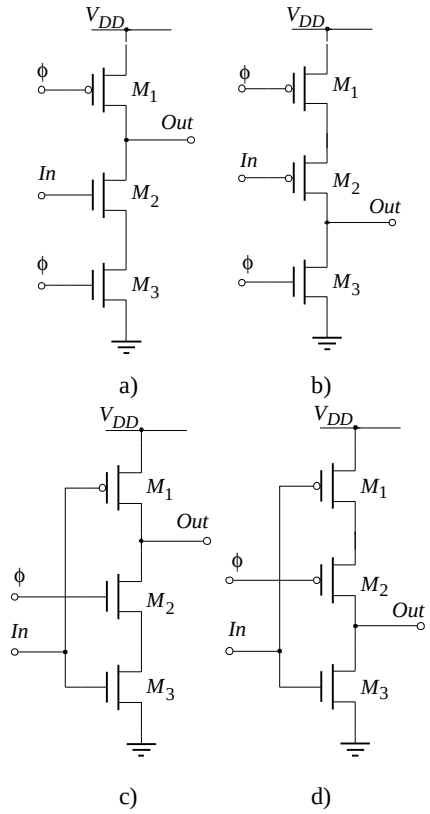

Figure 2. Basic CMOS TSPC stages:
a) precharged N, b) precharged P,
c) non-precharged N, d) non-precharged P.

2. NEW BICMOS LATCH

The biggest problem of the conventional BiCMOS circuits is their performance degradation at low supply voltages. The QC-BiCMOS inverter, proposed by Hitachi [4], overcomes that problem, without using a PNP transistor to restore the full swing. In this circuit, the PNP transistor is substituted by PMOS-NPN Darlington configuration, resulting in smaller dependence in pull-down operation of the circuit. This configuration has separate pull-up and pull down networks, thus the latch can be integrated in their CMOS parts.

TSPC technique is commonly used in high performance digital systems due to its simplicity and fast operation [3]. Four basic stages exist in TSPC, pre-charged N and P, and non-pre-charged N and P, as shown on Fig. 2.

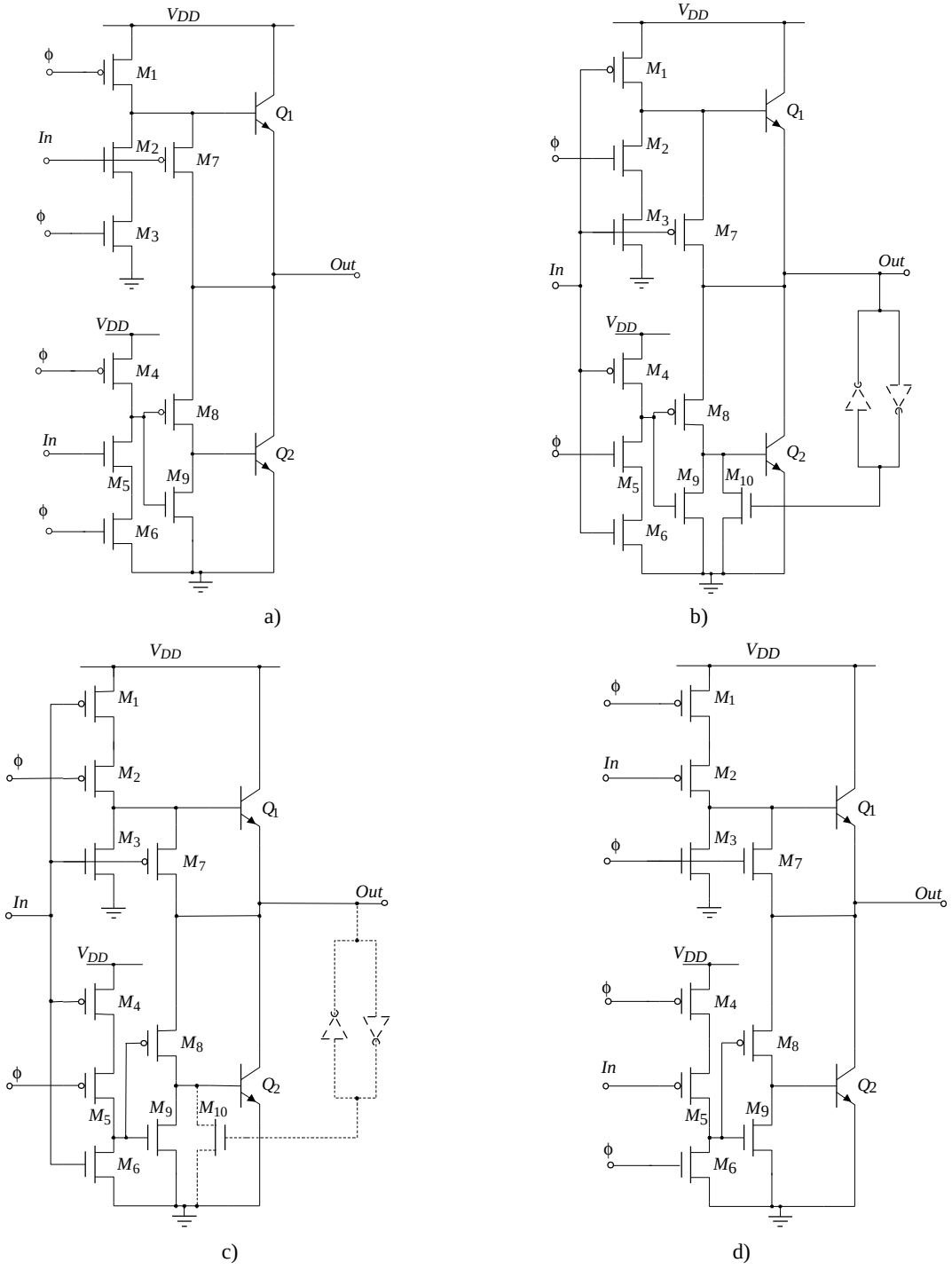

Figure 3. BiCMOS N-type TSPC stages:
a) N-type precharged, b) N-type non-precharged, c) P-type precharged, d) P-type non-precharged.

By combining these stages latches and flip-flops can be formed. For example, N type latch consists of two non-pre-charged N stages. However, driving capability of the CMOS implementation of the TSPC latch is limited and the latch itself is susceptible to noise. Our objective was to improve its driving capability and eliminate the floating nodes, which makes the proposed latch more robust and capable of driving very high fan-out nodes.

A. Latch operation

The new BiCMOS implementation of the TSPC N sections is shown on Fig. 3. a) and b). Pre-charged stage is shown in Fig. 3.a) and non pre-charged stage is shown in Fig. 3.b).

In Fig. 3.a) transistors M_1 - M_3 and M_4 - M_6 form the N-section of the CMOS pre-charged N stage in pull-up and pull-down networks. They pre-charge the transistor bases when $\phi = 0$ and perform logic evaluation when $\phi = 0$. The advantage of this design is that logic function blocks can be included in the latch, by placing them instead of M_2, and M_5 [3]. If this stage is preceded by other dynamic stages in the pipeline, transistor M_6 could be eliminated to speed-up the circuit operation [6].

In Fig. 3.b) transistors M_1 - M_3 and M_4 - M_6 form the N-section of the CMOS non-pre-charged N-stage. They are transparent when $\phi = 1$ and perform latching when $\phi = 0$. The transistors M_1, M_3, M_4 , M_6 could be replaced by a network implementing a logic function. Adding a single transistor as shown in [1], can eliminate the dynamic nodes in the circuit.

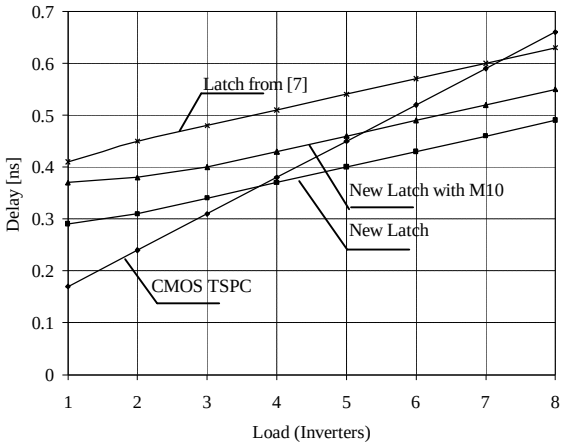

Figure 4. Delays from clock to output vs. load for a) new N type latch, b) new latch with M10, c) CMOS TSPC N latch, d) latch from [7].

Full latches and flip-flops can be designed by combination of CMOS and BiCMOS stages, in the way it is described in [3]. The BiCMOS part is based on original QC-BiCMOS, with additional improvement by replacing resistors by transistors M_7 and M_9, which is done in similar way as in [6]. By keeping the charge stored in the base of bipolar transistors they are biased to be off during the corresponding pull-up or pull-down operation, thus allowing steep transition until the output reaches the supply rail. Addition of transistor M_{10} together with cross-coupled inverters at the output improves rise and fall times [4, 6], but increases the propagation delays. These inverters also allow the latch to be used as fully static, and not only as a TSPC pipeline stage. In that case the logic level at the end of the clock phase is latched on the output node.

The P type sections are designed in similar way, by replacing the CMOS N sections with pre-charged or non-pre-charged P sections, as shown on Fig. 3 c) and d).

B. Circuit Performance

For the performance evaluation the N type latch consisting of the non-pre-charged CMOS N stage and non-pre-charged BiCMOS N stage is designed. The circuits are simulated using HSPICE in 0.5μm BiCMOS technology. All the transistors had minimal gate length of 0.5μ, NMOS transistors were 5μm wide and PMOS transistors were 10μm wide.

The loads used in all simulations that determine the driving capability were the CMOS inverters with W_p/W_n = 10μ/5μ, which had equivalent input capacitance of approximately 20fF.

The driving performance is compared to TSPC latch implemented in CMOS [3], and with the latch proposed in [7], with the same transistor sizes. The new latch is always faster and dissipates less power than latch published in [7], and is faster than CMOS implementation for fan-outs bigger than 3. The Fig. 4 shows the dependence of the average delay from clock input to the output for these circuits. The comparison is made fair by adjusting the input capacitance of all the circuits to be the same, as shown in [9].

The proposed circuits are suitable for use with a low power supply voltage which can be as low as 1.5V. The BiCMOS latch delay is smaller than its CMOS implementation at supply voltages from 1.5V to 5V, as shown on Fig. 5. The comparison is done with the load of eight inverters.

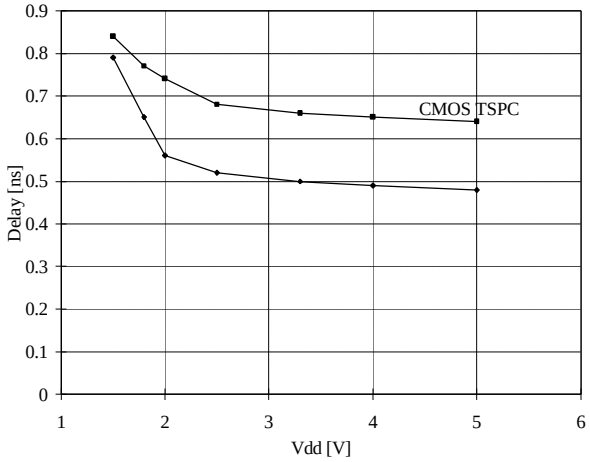

Figure 5. Comparison of BiCMOS and CMOS TSPC N stage delays having fan-out of 8.

This proposed BiCMOS latch has significant power savings compared to CMOS implementation for the fan-outs larger than 4. Fig. 6 shows the power consumption comparison between BiCMOS and CMOS stage with respect to the fan-out. The size of the second CMOS stage (in the CMOS latch) was increased (or decreased) proportionally until its delay was equal to that of BiCMOS latch. This is done in order to make the power comparison fair similar to [9]. The input stages of both stages

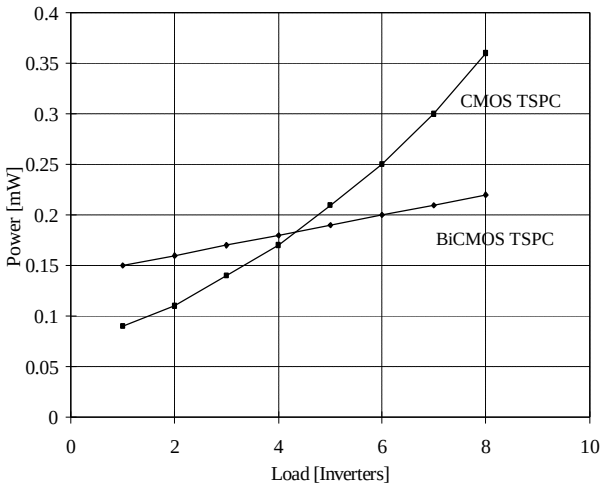

Figure 6. Power comparison of CMOS and BiCMOS implementations.

were unchanged. The reasons for this saving in power is that the bipolar transistors in the QC stage conduct current for a short amount of time, quickly charging/discharging the output node [4]. The CMOS stage needs significantly larger sizes of the transistors to achieve the same delay with bigger loads, which also increases the loading capacitance at the output and results in longer rise and fall times and increased DC current [10].

3. CONCLUSION

The advantage of the true single-phase clock design is significantly improved when the TSPC latch is implemented in BiCMOS. This paper proposed a new latch design and analyzed its performance. This design was obtained by combining TSPC CMOS and BiCMOS stage. The new latch is suitable for high performance systems that inherently produce larger fan-outs, thus requiring larger driving capabilities by utilizing short pipeline stages. It has smaller average delay than previously published circuits as well as smaller power dissipation. The advantages in speed and power over its CMOS counterpart are apparent when driving fan-outs larger than 4.

4. REFERENCES

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