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Synthesis of High-Speed Pass-Transistor Logic

Vojin G. Oklobdzija and Benoit Duchêne

***Abstract*—This brief presents new pass-transistor logic which contains fewer transistors and has better performance than Hitachi's double pass-transistor logic (DPL). The new logic is characterized by excellent speed and low power.**

***Index Terms*—CMOS, pass-transistor logic.**

I. Introduction

New CMOS logic using pass-transistor circuits has been proposed recently with the objective of improving speed and power consumption [2]–[4]. The double pass-transistor logic (DPL), developed by Hitachi demonstrated a 1.5-nS 32-bit ALU and 4.4-nS 54-bit multiplier in 0.25-μm technology [2], [4]. However, DPL has not yet been fully adopted because of its high transistor count. The logic proposed here minimizes the number of transistors used in DPL and preserves the speed. The simulations and tests were performed using 1-μm CMOS.

II. New Logic Gate

DVL (dual value logic) gate was obtained by eliminating the redundant branches and rearrangement of signals in DPL. Signal rearrangement results in NAND gate configuration which is faster than DPL (60 pS versus 75 pS), where the AND half is faster. These simplifications, illustrated in Figs. 1–3, preserve the advantages of DPL gates.

Finally, we chose a faster half from Fig. 1 and from Fig. 2. The resulting DVL gate contains total of eight transistors compared to DPL consisting of four transistors of each type. There is a total of nine inputs in DVL versus 12 in DPL resulting in a smaller capacitive load of DVL gate. In DVL, three inputs are connected to the transistor source and six to the gate (three to p-type and three to n-type). In DPL 4, inputs are connected to the source and eight to the gate (four to p-type and four to n-type transistors).

A similar method can be used to build the NOR/OR gates.

Comparison with CMOS: A comparison between DVL and conventional CMOS for given function $F_2 = \overline{BC} + AB\overline{C}$ is shown in Fig. 4 and in Table I.

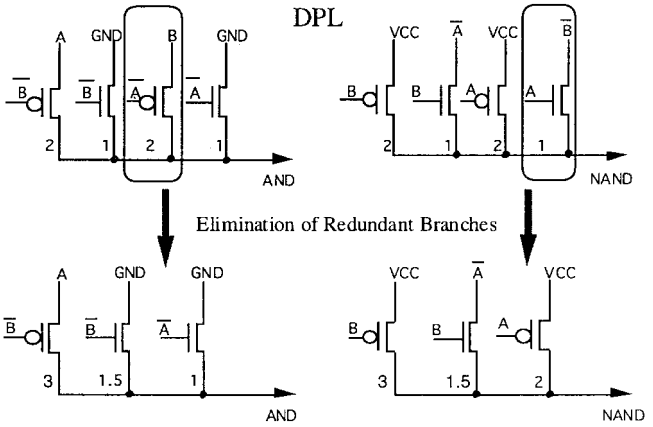

Fig. 1. Elimination of redundant branches.

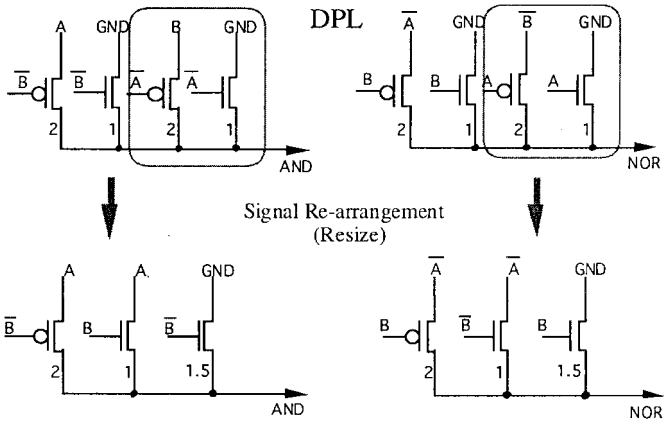

Fig. 2. Signal rearrangement.

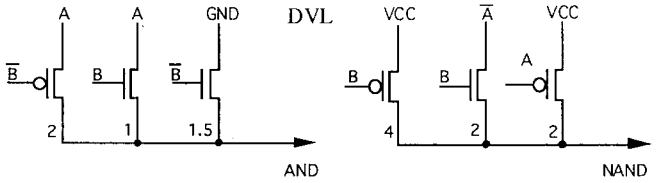

Fig. 3. Resulting DVL gate.

TABLE I
Comparison Between DVL and CMOS

Function F2	CMOS	DVL	Savings
No. of Transistors	10nMOS 10pMOS	8pMOS 8nMOS	20%
No. of Levels	3 gate levels	2 transistor levels	
Global size	44	36	18%
Delay @ 50% of Vout	430pS	245pS	43%
Transitor ratio	Wp/Wn=2	Wp/Wn=2	

Manuscript received June 10, 1995; revised November 12, 1995. This paper was recommended by Associate Editor S. Kiaei.

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Publisher Item Identifier S 1057-7130(97)07654-4.

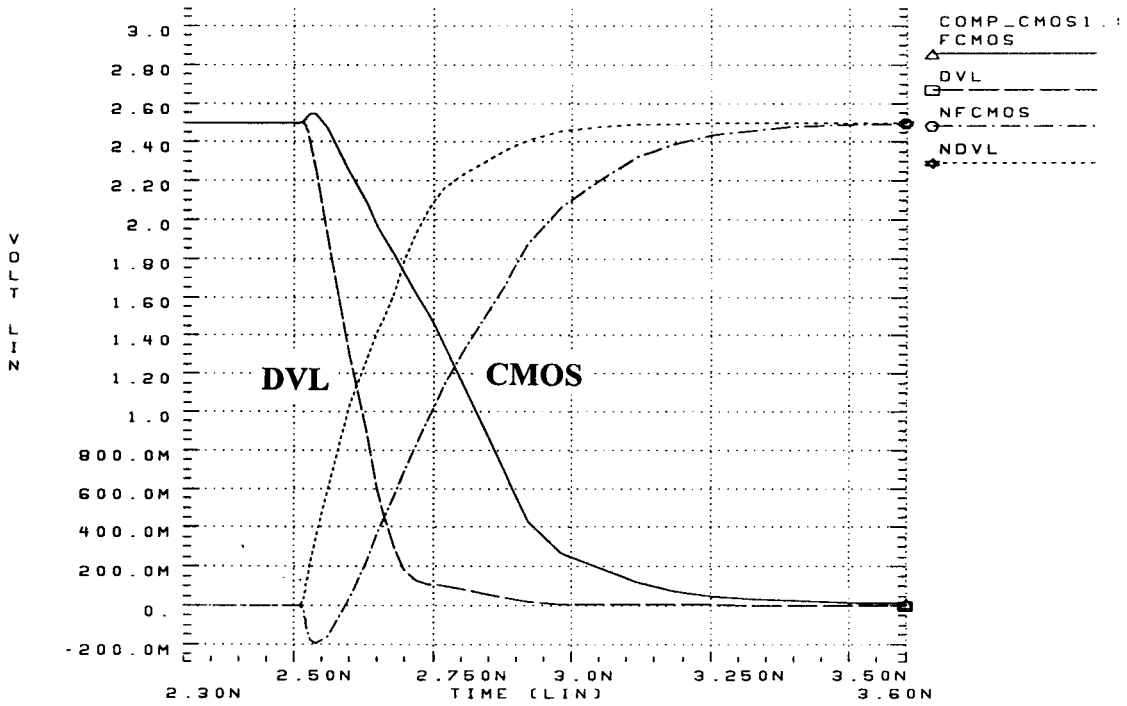


Fig. 4. Delay comparison between DVL and conventional CMOS for a three inputs function F_2.

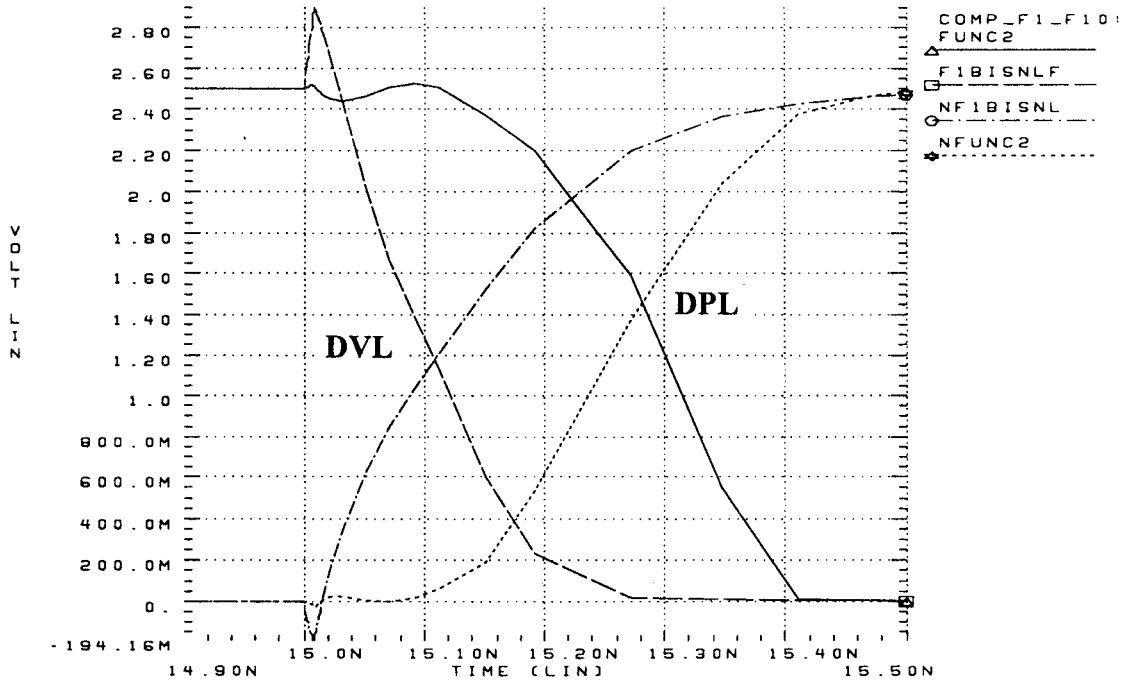


Fig. 5. Simulated delays for the three inputs DPL function F_2 and DVL implementation of F_2.

Comparison with DPL: The function F_2 used for comparison was implemented using four DPL gates in two logic levels. Afterwards, this circuit was built using the DVL. The load applied to the o utput is a standard load of two gate inputs.

Comparison with CPL: The function F published by Yano in [1] was synthesized for DVL and compared to CPL which uses lean cells and special inverters [3]. Delays were measured for 1 cell, 2 cells, and 3 cells cascaded. DVL circuit is made with conventional inverters.

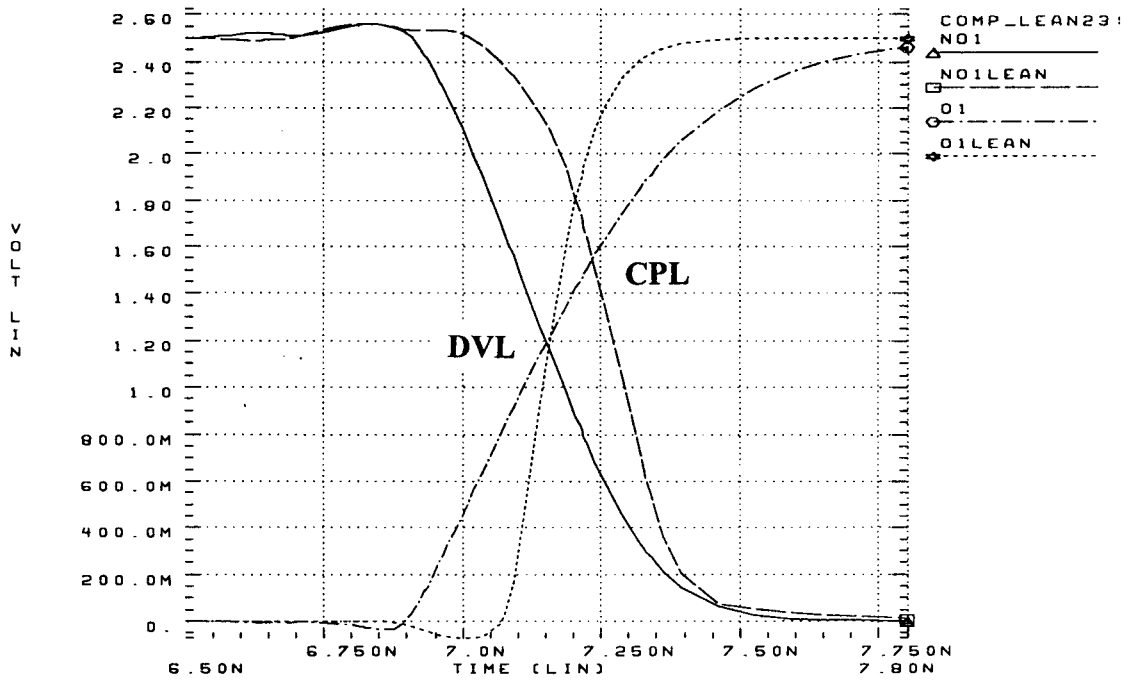
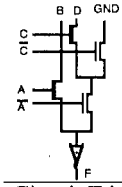


Fig. 6. Delays comparison between two cascaded DVL and CPL cell.

TABLE II
COMPARISON BETWEEN DPL AND DVL

Function F2	DPL	DVL	Savings
No. of Transistors	16pMOS 16nMOS	8pMOS 8nMOS	50%
No. of Levels	2 gate levels	2 transistor levels	
Global size	48	30	37.5%
Delay @50%	290pS	120pS	58.6%
@80%	350pS	240pS	31.4%
Transistor ratio	Wp/Wn=2	Wp/Wn=2 2 nMOS=1.5	

TABLE III
COMPARISON BETWEEN CPL AND DVL

	1 cell	2 cells	3 cells	Cell size
	375pS (100%)	760pS (100%)	1,150pS (100%)	105μ (100%)
Circuit F in DVL	380pS (101%)	660pS (86%)	950pS (82%)	108μ (103%)

The comparisons were made using the output load of 150 fF in both cases (Table III and Fig. 6).

III. CONCLUSION

A DVL logic family, which has advantages over standard CMOS as well as new pass-transistor families, has been developed. Generation of DVL is supported by an automated synthesis tool based on the algorithm developed in the course of this brief.

ACKNOWLEDGMENT

The authors acknowledge the contributions of P. Lee, W. Wong, and H. Yu.

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