Design and Experimental Verification of a CMOS Adiabatic Logic with Single-Phase Power-Clock Supply

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Abstract¾ A new adiabatic CMOS logic that operates from a single-phase power-clock is presented. A simple and efficient power-clock generator is integrated with the logic to generate the required AC power-clock supply waveform. Circuit performance is evaluated using a chain of inverters realized in 1.2mm technology. Experimental results show energy savings comparable to other adiabatic logic families that require multi-phase power-clocks.

I. Introduction

Low energy operation is a must in many of today's digital systems. The classical approaches to achieve low-energy computation are in reducing the supply voltage, reducing the loading capacitances of the gates or reducing the activity factors (number of input transitions).

The alternative approach for energy savings is in energy-recovery (or 'adiabatic') circuits, which has been examined using various circuit implementations [1-11]. Weaknesses of the previously proposed approaches include the need for multi-phase AC power-clock supplies for proper interfacing between stages, with correspondingly high complexity of both the logic and the required power-clock generator [1-9].

This paper describes the design and the results of experimental evaluation of the clocked adiabatic logic (CAL) [10,11] operated from a single-phase power-clock generator integrated with logic [11]. The measurements are focused on verification of operation of the logic over frequency and supply voltage ranges and a comparison of CAL energy consumption to the case when the logic is operated from a DC power supply.

CAL circuit configuration and operation are described in Section 2. Implementation issues and the test chip are discussed in Section 3. Measurement results are presented in Section 4. Section 5 concludes the paper.

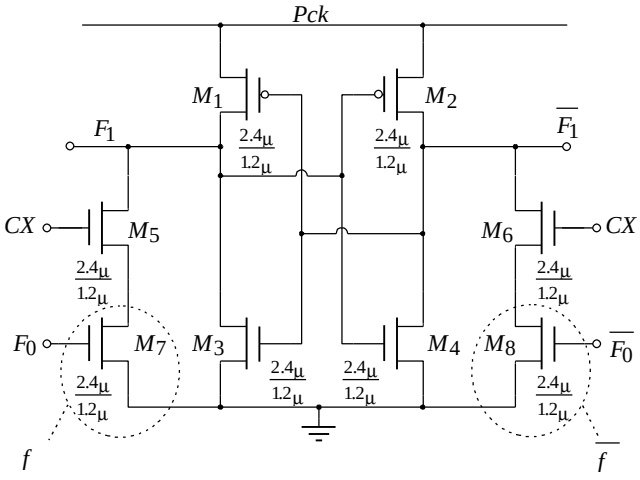

Fig. 1: CAL inverter.

II. Circuit operation

The basic CAL gate, the inverter, is shown in Fig. 1. Cross-coupled CMOS inverters, transistors M_1-M_4, provide the memory function. In general, the devices M_7 and M_8 can be replaced with NMOS logic trees to perform switching involved in the evaluation of an arbitrary binary function. Fig. 1 shows that M7 should be replaced by the transistor tree that evaluates the true logic function, while the tree that replaces M8 should implement the complementary function. The CAL topology and operation are similar to the logic proposed by Denker [6]. Our innovation is the inclusion of path control switches, devices M_5 and M_6, added in series with the logic trees. This modification allows operation of the circuit with a single-phase power-clock supply, *Pck*, as opposed to the four-phase power clock required by the logic proposed in [6]. Compared to multi-phase operation, single-phase power clock operation allows simple power clock generation, resulting in power savings in the clock generator.

Idealized CAL timing waveforms for the inverter are shown in Fig. 2. The power clock *Pck* is shown as a trapezoidal waveform. Logic evaluation is enabled by the auxiliary clock *CX*. For $F_0 = 0$, M_7 is off, M_8 is on, the

complementary output $\overline{F_1}$ goes to 0, and the true output F_1 follows the power-clock waveform. In the next clock period, the auxiliary clock $CX = 0$ disables the logic evaluation and the outputs repeat the result stored during the evaluation in the previous clock period. As a result, the CAL logic states are represented by presence or absence of a pair of pulses. When controlling a chain of logic stages, the same power clock *Pck* supplies all CAL stages. The logic evaluation is enabled in alternate logic stages by the auxiliary clock *CX* and its complement $\overline{CX}$. To reduce power consumption in the auxiliary clock distribution, the swing of the auxiliary clocks can be reduced without affecting the signal levels in the logic. It is interesting to note that CAL can also be operated as a conventional clocked logic with a DC power supply connected to *Pck*.

III. Implementation

Fig. 3 is a block diagram of the experimental CAL chip built as a chain of $n = 736$ dual-rail inverters in 1.2μm CMOS technology. The device sizes in the CAL logic stages are indicated in Fig. 1 and Fig. 3. For testing purposes, twelve of the inverters have both outputs connected to the output pins, via conventional output buffers that serve as voltage comparators. The conventional output buffers and the circuits used to generate the auxiliary clocks are supplied from a separate DC supply V_{DD}. The inductor *L* and the low-voltage DC source V_B are used for energy-recovery (adiabatic) operation of the CAL chip. The AC power-clock waveform *Pck* is generated using a single NMOS device *Q* in parallel with the CAL logic. The device *Q* is turned on during a small fraction of the clock period at the point when *Pck* is approximately zero. During this time, energy is added to sustain oscillation in the resonant circuit formed by the external inductance L and the equivalent logic capacitance C_{eq}. When *Q* is clocked close to the resonant frequency, *Pck* swings between *0* and a peak value approximately equal to $2 \cdot V_B$ [11]. The switching transistor *Q* takes a small fraction of the total chip area.

Given a desired power-clock frequency *f*, the required inductance *L* can be found from

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}},$$

where $C_{eq} = 101\text{pF}$ is the measured equivalent chip capacitance at the *Pck* node. The equivalent chip capacitance was measured by connecting a resistor *R* between V_B and *Pck* and by measuring the time constant RC_{eq} of the charge-up transient after the device *Q* is turned off. The logic can also be operated from a DC supply connected directly to *Pck*, while the power-clock device *Q* is disabled. This non-adiabatic mode of operation is used to evaluate how much energy can be recovered by the power clock.

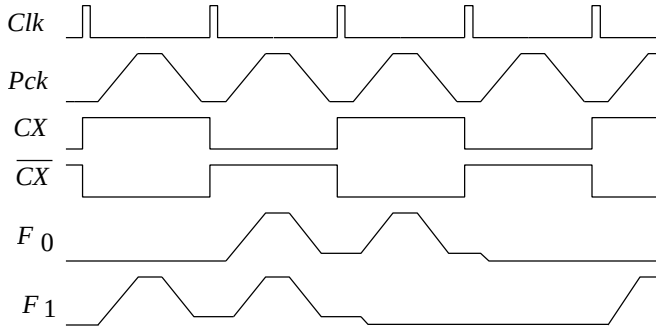

Fig. 2: Idealized CAL timing waveforms.

IV. Experimental Results

Operation of the circuit is illustrated by the waveforms shown in Fig. 4 for an input sequence of 1100 at the operating frequency $f = 2.36\text{MHz}$. The logic was supplied from $V_B = 1.5\text{V}$ and the DC supply of the output buffers was $V_{DD} = 5\text{V}$. The pair of quasi-sinusoidal pulses that corresponds to the logic high output is observed as a pair of rectangular pulses through the conventional, DC-supplied output buffers. The maximum operating frequency of the circuit in this test configuration was 50MHz, due to signal

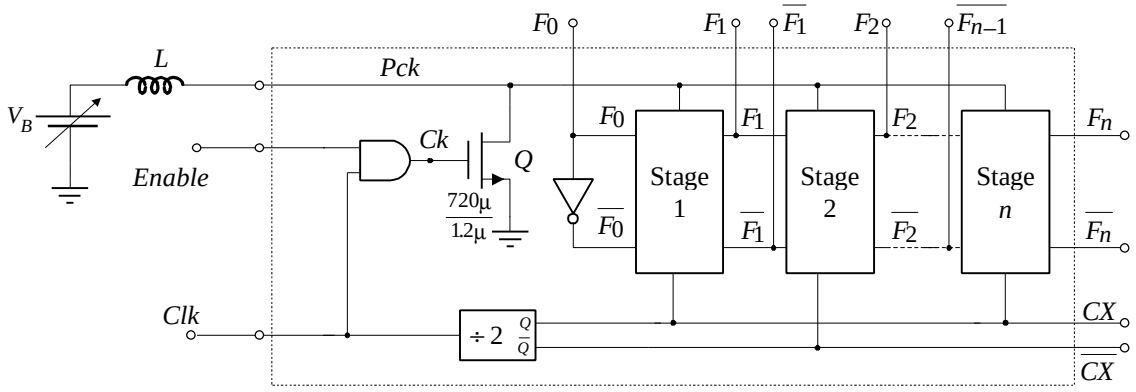

Fig. 3: A chain of CAL logic gates with on-chip power-clock generation. For adiabatic operation, *Enable* = 1, and inductor *L* is connected between *Pck* and the DC supply V_B; for non-adiabatic operation, *Enable* = 0 and *Pck* = V_B.

source limitation. Higher operating frequencies are predicted by simulation [10].

Energy consumption of the CAL chip (excluding the consumption of the output buffers) was measured as a function of frequency for three cases:

1. For adiabatic operation when 3V peak-to-peak sinusoidal *Pck* was supplied from an external function generator and the on-chip power-clock device *Q* was disabled.

2. For adiabatic operation with quasi-sinusoidal *Pck* generated using $V_B = 1.5$V and an external *L*, and by clocking *Q* as shown in Fig.3.

3. For non-adiabatic operation with the minimum DC supply voltage $V_B = 2.5$V for which the DC-supplied logic was found to function properly.

In all three cases, the activity factor (defined as the normalized number of input transitions) is equal to 1. The results for power consumption per inverter are shown in Fig. 5. Fig. 6. shows energy consumption per cycle per inverter. The non-adiabatic energy consumption is approximately constant at 0.58pJ per inverter per cycle. The theoretical non-adiabatic energy consumption, based on the measured $C_{eq} = 101$pF is 0.61pJ per inverter per cycle. The small difference comes from the fact that C_{eq} includes capacitance of the *Pck* distribution, which is not switched during non-adiabatic operation. These results show that the energy consumption of the CAL operated from the DC supply is indeed equal to CV^2 losses. Therefore, the results of Fig. 6 show how much of the CV^2 can be recovered through the power clock during adiabatic operation of the chip with external or internal power clock. Energy savings are very large at low operating frequencies and diminish as the frequency approaches $f = 30$MHz. The results with the externally supplied power-clock waveform are significantly better than the results with the internally generated *Pck*. We believe that significantly better performance of the internal power-clock generator can be obtained by increasing the size and reducing the on-resistance of the switching transistor *Q*.

By changing the activity factor at a constant power-clock frequency it was found that the CAL power consumption at the activity factor equal to 0 is approximately one half of the power consumption at the activity factor equal to 1, as shown in Fig. 7. This confirms that at low activity factors non-adiabatic operation from a DC supply can be significantly more efficient.

The CAL ability to operate from either a single-phase AC power-clock supply or from a DC supply opens interesting possibilities to combine adiabatic and non-adiabatic modes of operation to achieve energy-efficient operation for a very wide range of throughput rates and activity factors.

The power and energy consumption measurements shown in Figs. 5, 6 and 7 included only the part of the circuit operated from the supply V_B – the logic and the switching transistor *Q*. The measured energy consumption per cycle of the circuits supplied from the constant DC voltage $V_{DD} = 3$V (auxiliary clocks and the driver for the switching transistor *Q*) is about 30pJ, or about 8% of the total non-adiabatic energy consumption.

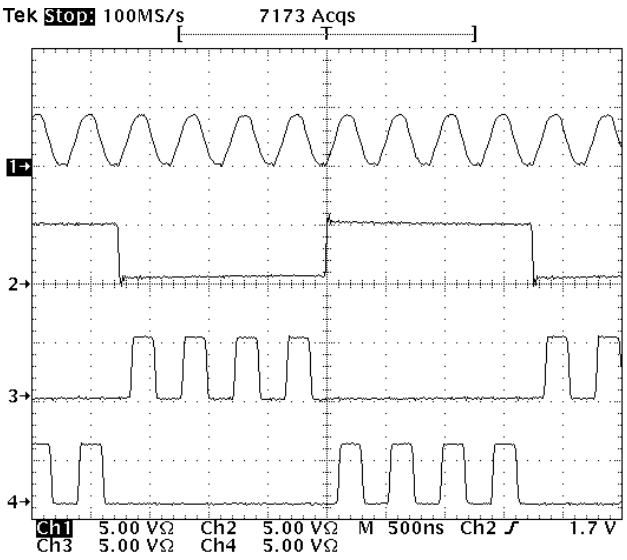

Fig. 4: Measured CAL waveforms:
Ch1: power clock *Pck*, Ch2: logic input F_0, Ch3: buffered logic output F_1, Ch4: buffered complementary logic output $\overline{F_1}$.

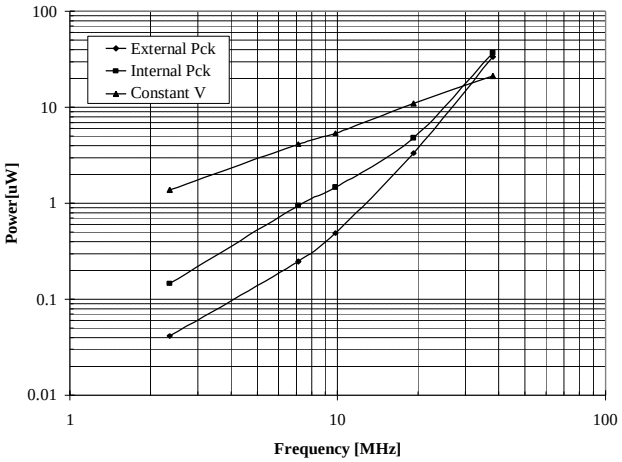

Fig. 5: Power per inverter vs. frequency

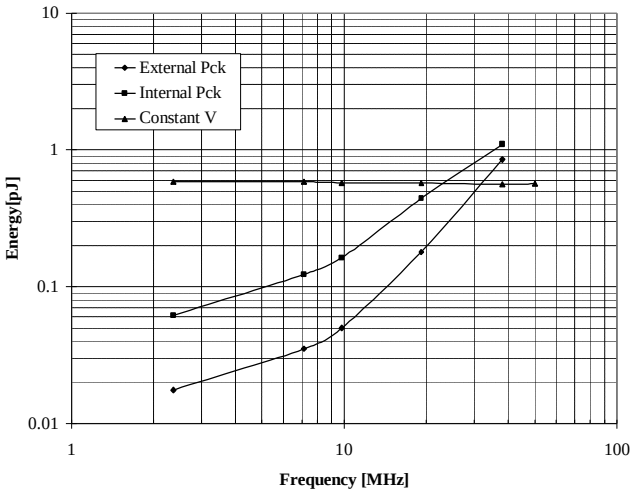

Fig. 6: Energy/inverter per cycle vs. frequency.

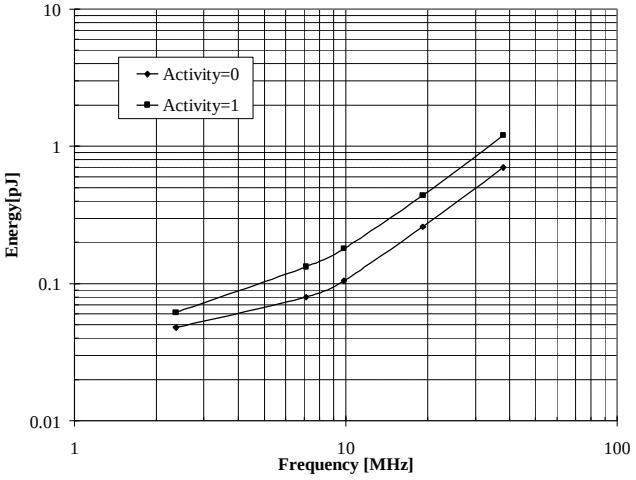

Fig. 7: Energy/inverter vs. frequency for different activity factors.

V. Conclusion

The proposed clocked adiabatic logic (CAL) operates from a single-phase power-clock supply. The test chip, consisting of a chain of inverters, is implemented in a 1.2μm CMOS technology. Operation of the logic and its energy consumption are measured for adiabatic operation using an external power-clock generator or using a simple on-chip power-clock generator. These results are compared to the energy consumption measured in non-adiabatic operation when the chip is supplied from a DC voltage source. Experimental results show significant energy savings at relatively low clock rates. The CAL ability to operate from either AC power-clock supply or from a conventional DC supply opens further possibilities for energy-efficient operation in a very wide range of throughput rates by combining adiabatic and non-adiabatic modes of operation.

Acknowledgments

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