Circuit Sizing and Supply-Voltage Selection for Low-Power Digital Circuit Design

Milena Vratonjic, Bart R. Zeydel, and Vojin G. Oklobdzija

Department of Electrical and Computer Engineering,
University of California, Davis, CA 95616
{milena, zeydel, vojin}@acsel-lab.com
http://www.acsel-lab.com

Abstract. This paper analyzes energy minimization of digital circuits operating at supply voltages above threshold and in the sub-threshold region. Circuit sizing and supply-voltage selection are simultaneously analyzed to determine where the minimum energy solution occurs. In this work we address the effects of architectural modifications on the design choices in different regions of operation. Two new architectural parameters are introduced that can be used for fast design comparison in the low power region of operation.

1 Introduction

Modern wireless handheld devices utilize signal processing algorithms with complex computational demands, requiring hardware implementations that support high-speed computing yet maintain low-power levels. To extend battery life, the optimal design for these devices is the one which achieves the lowest energy consumption at the desired performance target. In order to find the optimal design, circuit designers must understand the impact of circuit sizing, supply voltage and technology limitations on the energy and delay of their designs.

In the fields of sensor networks and medical devices, speed is not as important as energy consumption. Reducing the amount of energy per computation allows for extended operation or smaller form factor. For ultra-low power, circuit designers have proposed operating with sub-threshold supply voltages.

This paper analyzes how circuit sizing and supply voltage should be used to achieve minimum energy consumption at the desired performance. Two design approaches are used: (1) starting from the highest-performance point (Logical Effort [7]) we show the best way to trade delay relaxation for energy reduction; (2) from the point corresponding to the minimum sizing of the circuit, we show how up-sizing, supply-voltage scaling and architectural modifications lead to the best trade-offs in energy and delay.

Finally, we introduce two architectural parameters which can be used to quickly find the most energy-efficient circuit design.

J. Vounckx, N. Azemard, and P. Maurine (Eds.): PATMOS 2006, LNCS 4148, pp. 148 – 156, 2006.

2 Energy Components

The total energy consumption of a circuit can be expressed as the sum of three components: dynamic energy (E_{dyn}), short-circuit energy (E_{sc}) and leakage energy (E_{lkg}). Until recently, dynamic energy dominated energy consumption in digital circuits. However, as CMOS technology advances into sub-100nm, leakage energy is becoming as important as dynamic energy.

Short-circuit, or so-called crowbar current, occurs only when both pMOS and nMOS are conducting at the same time. For low supply-voltage values, when $V_{dd} < 2V_T$, short-circuit energy component is eliminated. When supply-voltage falls below the threshold voltage, V_T, we enter the sub-threshold region of operation where the transistor current is given by:

$$I_{sub} = I_{off} e^{(V_{GS}-V_T)/nV_{th}}, I_{off} = \mu_o C_{ox} \frac{W}{L}(n-1)V_{th}^2 \quad (1)$$

with n corresponding to the sub-threshold slope and V_{th}=kT/q.

3 Optimization for Minimum Energy

In this section we examine the optimization of circuit sizing and supply voltage selection to minimize energy at a desired performance target. For analysis we use a 130nm technology with a fixed threshold voltage (V_T). The optimization process is therefore reduced to the design space exploration for finding circuit sizing and supply-voltage. It was shown previously in [2] how balancing sensitivities of a design to the sizing and supply-voltage gives the optimal solution on the energy-efficient curve.

3.1 Circuit Sizing

Dynamic energy is directly proportional to the equivalent switched capacitance at the output of the logic gate:

$$E_{dyn} = \alpha C_{tot} V_{dd}^2 \quad (2)$$

where α is activity factor and C_{tot} is the total gate capacitance (total transistor width). Mathematically and intuitively from equation (2), the minimum sized circuit would provide the minimum energy point. This is the case when the supply-voltage is above the threshold voltage. The solution becomes less obvious at the sub-threshold region of operation where minimum sized devices have failure point at higher supply-voltages comparing to the devices sized-up for functionality at lower supply-voltages. It was shown in [1] that due to the shallow nature of the optimum point corresponding to the energy minima, reaching the minimum possible supply-voltage through the up-sizing of the devices does not allow for any significant energy savings comparing to the minimum sized solution. Therefore, using minimum sized devices is a good approach when designing in the sub-threshold region.

It was shown by Zyuban et. al [2] that every design point on the energy-efficient curve obtained through the circuit sizing corresponds to the certain value of hardware intensity (η). Hardware intensity is defined as the percentage of energy increase per percentage of delay improvement on the energy-efficient curve attainable through the circuit sizing. At the point where this percentage corresponds to the value of 1%, the hardware intensity (η) equals to one and this is indeed the energy-delay product (EDP) point.

A good starting point for circuit sizing is the delay optimized sizing of a circuit for a fixed input size and output load using Logical Effort [7] (LE point). There are two possible approaches to lowering energy consumption of the circuit starting from LE point: 1) if it is allowed to increase the input size of the circuit, the techniques proposed in [3] give solution for energy minimization by redistributing the stage efforts among the stages and keeping the delay fixed at lower energy level; 2) if change in input is not possible, we can trade the delay increase by either circuit sizing or through the use of lower supply-voltages.

3.2 Supply-Voltage Scaling

Supply-voltage reduction is often considered the most effective technique for low-power design. Similar to the hardware intensity, we can express voltage intensity (θ) as the tradeoff between the energy and delay of the circuit due to the supply-voltage, as shown by Zyuban et. al [2].

As supply-voltage decreases, total energy decreases until the sub-threshold region is reached. In the sub-threshold region, propagation delay increases exponentially with respect to supply-voltage reduction resulting in diminishing returns in energy savings due to the increase in leakage energy. Therefore, minimum voltage operation point does not coincide with the minimum energy point. Minimum energy point occurs at the supply-voltages higher then the minimum supply-voltage points where the design is still operational.

3.3 Minimum Circuit Sizing with Supply-Voltage Scaling

Recently, we have shown that more complex high-performance structures combined with supply-voltage scaling outperform traditional low-power oriented designs in the low- and ultra-low power domains [4]. The designs were sized for minimum energy

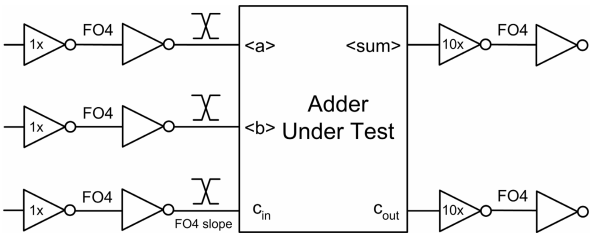

Fig. 1. Simulation test bench

operation such that the minimum energy point is initially obtained through the minimum circuit sizing and then supply-voltage was varied from 1.2V to 0.6V.

The results are obtained from simulations in a 130nm technology under nominal process conditions. The simulation test bench is shown in Figure 1.

Fig. 2. shows the voltage intensity, θ, and energy of the minimum sized Sparse Carry-Lookahead adder design (SCL) [4, 5] with supply-voltages scaled below 0.6V. The adder is functional in sub-threshold voltage region even at 0.1V (the threshold voltage is 220mV in the 130nm technology used for analysis).

It is also shown in Fig. 2. how the voltage intensity of the design changes as supply-voltage is varied. The point where no further savings in energy is possible through supply-voltage reduction (E_{min}) corresponds to the supply-voltage for which the voltage intensity is zero.

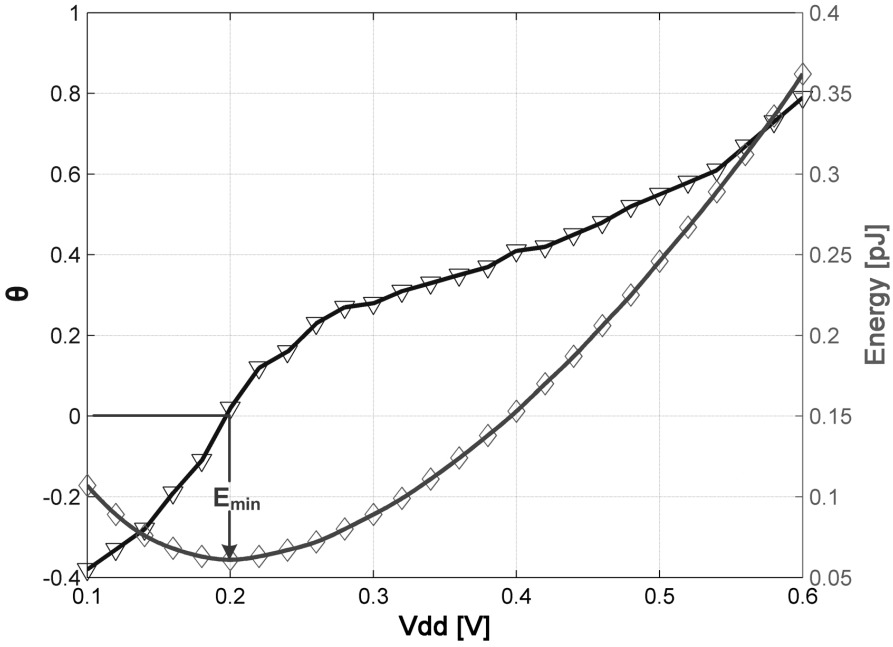

Fig. 2. Energy-Delay curve of the minimum-sized Sparse Carry-Lookahead adder (SCL) with supply-voltages scaling from 0.6V to 0.1V

The minimum energy operation point occurs in the sub-threshold region at 0.2V (Figures 2, 3). The effect of supply-voltage on the energy and delay of the minimum-sized Sparse Carry-Lookahead Adder (SCL) and Ripple-Carry Adder (RCA) is plotted in Figure 3, for supply-voltages ranging from 0.6V to 0.1V. The two examples, SCL and RCA, are representatives of high-performance and low-power designs.

Dynamic energy consumption of a design depends on the size and switching activity of the circuits; while leakage energy depends on the size of the circuits and the cycle time. Design with fewer devices and longer cycle time (such as RCA adder) can

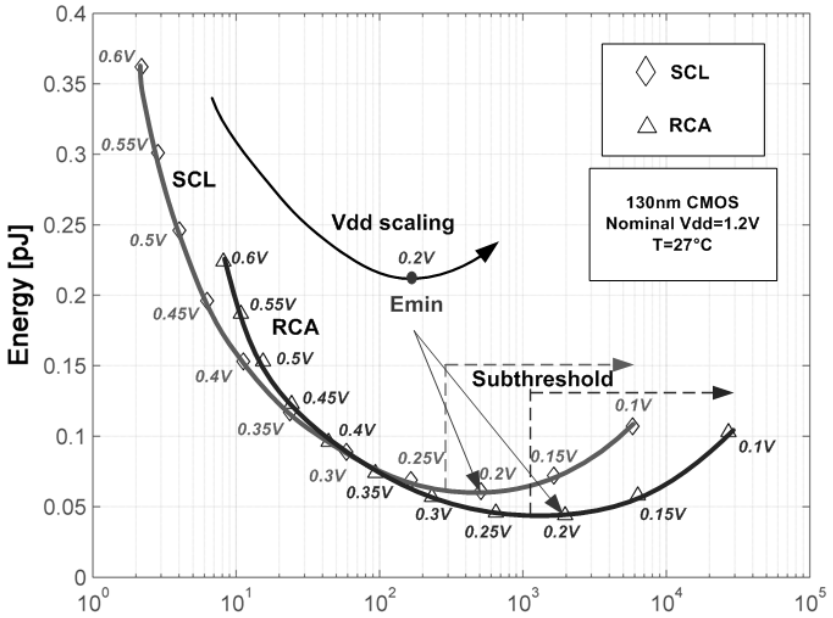

Fig. 3. Minimum Energy point at Sub-threshold operation

have more energy then a design which is faster and yet with more gates (such as SCL), Figure 3. For both of these designs, the minimum energy point occurred at supply-voltage of 0.2V, where the threshold voltage was 220mV.

In the next section, we show that the minimum sizing design approach does not provide the most energy-efficient solutions in cases where the performance target is greater then the minimum energy performance.

3.4 Simultaneous Device Sizing and Supply-Voltage Scaling

There exist two ways for circuit designers to achieve minimum energy solution. The first is to obtain Logical Effort (delay optimized sizing) and the second is to use all minimum sized circuits (energy minimized sizing). These two points correspond to the left and right ends of the minimum energy-delay bound (curve) for the solution space obtained from circuit sizing. The minimum energy points on this curve can be obtained by either down-sizing the circuit from the LE point or up-sizing the circuit from minimum sizes. Down-sizing from LE is most effective for performance targets near the LE solution, while upsizing from minimum is better to apply for slow performance targets. Minimum energy-delay curves of the Sparse Carry-Lookahead adder (SCL) for supply voltages 1.2V, 1.1V, and 1V are shown in Figure 4. The points on each curve are obtained by minimizing energy through circuit sizing from the LE point to the minimum size limit.

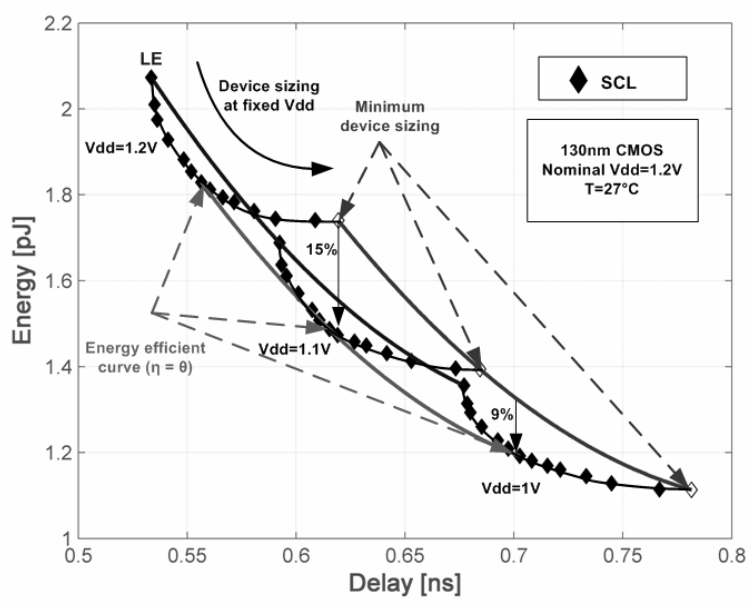

Fig. 4. Energy-Delay curve obtained through sizing and supply-voltage scaling

The minimum energy for each performance target is obtained by jointly optimizing circuit sizing and supply voltage. A compound energy-delay curve is created by selecting the minimum energy points from the combined energy-delay curves. At each of these points on the compound energy-delay curve hardware and voltage intensities are balanced [2]. If, for example, we need to meet the performance target of 0.62ns we have the following choices: using minimum sizing of SCL at nominal voltage of 1.2V, or reducing the supply-voltage to the value of 1.1V and up-sizing the design to meet the target performance. As seen from Figure 4, the second design approach results in 15% energy saving compared to the minimum sized SCL design at nominal voltage. If our performance demands were not so severe, i.e. delay is increased, we see that the energy savings decrease from 15% at 0.62ns to 9% at 0.7ns until the point where further voltage reduction and upsizing of the devices would not provide additional savings. This is the region where minimum sizing of the devices is the correct approach for reducing energy while still meeting the target performance.

4 Choices for Energy-Delay Optimization

In this section we investigate the consideration of different topologies in combination with device-sizing and supply-voltage scaling for energy-delay optimization.

Figure 5. illustrates example of two different adders as test cases, Variable-Block Adder (VBA) [6] and Ripple-Carry Adder (RCA) over a range of supply-voltages.

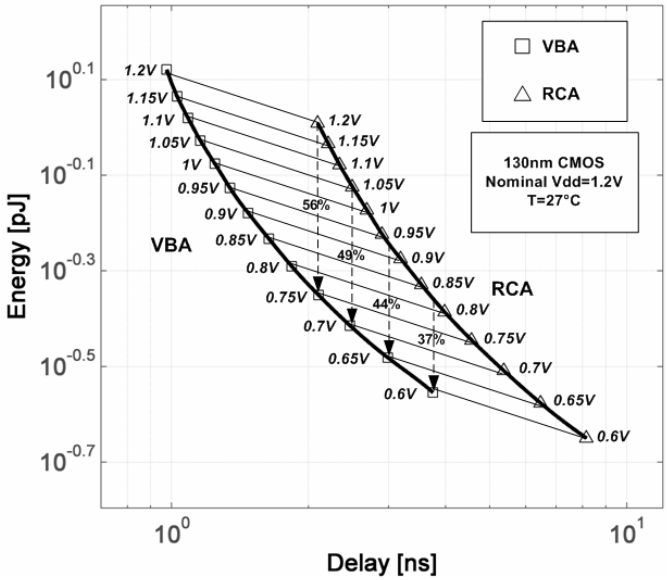

Fig. 5. Two different adders and corresponding energy savings at iso-performance with supply-voltage scaling @ minimum sizing

At the low-power region where the performance target is met even with the simplest and slowest topology, such as RCA is, using more complex structures at reduced supply-voltage levels results in significant energy savings, 56% at 2ns up to 37% at 3.8ns target delay. To expand on this analysis, we were interested in analyzing the relative energy-delay relationship of complex circuits over the wide range of supply-voltages.

We use the property of the constant energy-delay relationship versus supply-voltage observed in complex circuits [2, 3] to explore the tradeoffs between different designs. This property is not satisfied at lower supply-voltages where leakage energy is comparable to the dynamic energy consumption, Figure 3, and where the designs have cross-points in the energy-delay space.

The lines in Figures 5 and 6 connect the design points of the two topologies at iso-voltage. In the figures it can be seen that the relationship between the circuits remains constant, thus each circuit behaves the same with supply voltage. We use this property to introduce two new parameters, λ and ρ, that we are defining here as:

$$\lambda = \sqrt{\partial e^2 + \partial d^2}, \text{ where } \partial e = const \text{ and } \partial d = const \ @ \ \forall \text{ Vdd} \tag{2}$$

$$\rho = \tan\frac{\partial e}{\partial d}, e = \log E, d = \log D \tag{3}$$

Knowing these two parameters and the data-sets of one topology, {(D_1',E_1'), (D_2', E_2'), … , (D_k', E_k')}, we can easily obtain the design points of the second topology, {(D_1'',E_1''), (D_2'', E_2''), … , (D_k'', E_k'')}, for k-values of supply-voltage, which can then be used for quick design space exploration, eq. (4).

$$D_i'' = D_i' 10^{\frac{\lambda}{\sqrt{1+\rho^2}}},\ E_i'' = E_i' 10^{-\frac{\lambda\rho}{\sqrt{1+\rho^2}}},\ i=1, \ldots, k \tag{4}$$

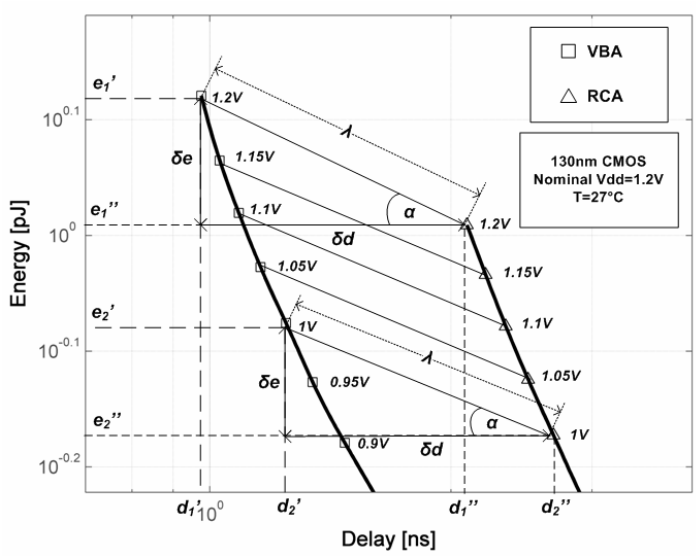

Fig. 6. Introducing parameters λ and ρ

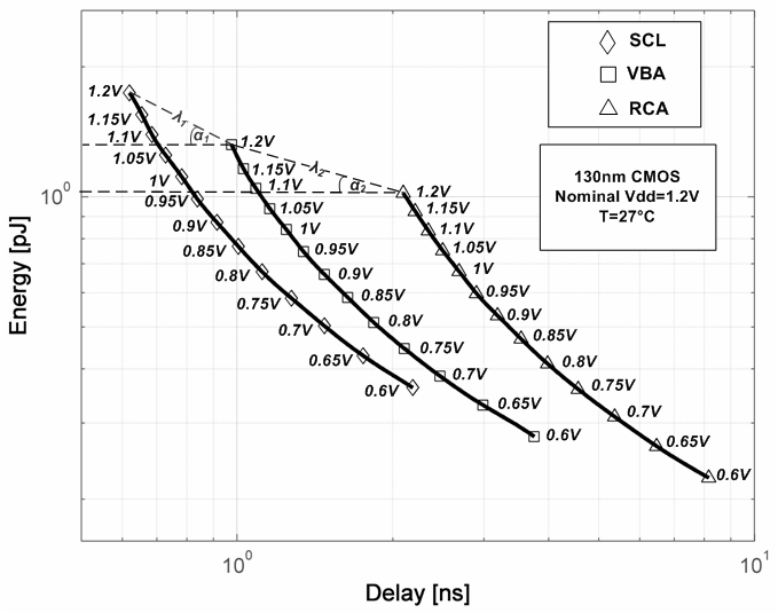

Fig. 7. Design space exploration with different adder topologies

Above defined parameters could be found based on the (E, D) points at nominal supply-voltage values. Knowing how one design behaves with the supply-voltage scaling, we can obtain the whole set of data points for a different one. Presented in Figure 7. are the data-sets of three topologies obtained from SCL data-set and, knowing parameters (λ_1, ρ_1) and (λ_2, ρ_2), data-sets are derived for VBA and RCA adders respectively.

5 Conclusion

This work demonstrates the importance of the joint optimization of supply-voltage and circuit sizing and proper topology for achieving minimum energy at the desired performance target.

Careful selection of supply-voltage, circuit sizing and topology simultaneously has bigger energy savings, compared to the case when they are taken in isolation. In the low-power region, operating at or around threshold voltage using minimum sized devices achieves the minimum energy solution. Below this point, supply-voltage reduction and circuit sizing do not provide further energy savings.

Acknowledgements

This work has been supported by IBM, SRC Research Grant No. 931.001, California MICRO, Fujitsu Ltd. and Intel Corp.

References

1. B. H. Calhoun, A. Wang, A. Chandrakasan, “Modeling and Sizing for Minimum Energy Operation in Subthreshold Circuits”, IEEE Journal of Solid-State Circuits, Vol. 40, No. 9, pp. 1778-1786, September 2005.
2. V. Zyuban, P. N. Strenski, “Balancing Hardware Intensity in Microprocessor Pipelines”, IBM Journal of Research and Development, Vol. 47, No. 5/6, 2003.
3. H. Q. Dao, B. R. Zeydel, V. G. Oklobdzija, “Energy Optimization of Pipelined Digital Systems Using Circuit Sizing and Supply Scaling”, IEEE Transactions on VLSI Systems, Vol.14, No. 2, pp. 122-134, February 2006.
4. M. Vratonjic, B. R. Zeydel, V. G. Oklobdzija, “Low- and Ultra Low-Power Arithmetic Units: Design and Comparison”, Proceedings of the International Conference on Computer Design, ICCD, San Jose, California, October 2-5, 2005.
5. S. Mathew, et. al, “A 4GHz 130nm Address Generation Unit with 32-bit Sparse-Tree Adder Core”, IEEE Journal of Solid-State Circuits, Vol. 38, No. 5, pp. 689-695, May 2003.
6. V. G. Oklobdzija, E. R. Barnes, “Some Optimal Schemes for ALU Implementation in VLSI Technology”, Proceedings of the Symposium on Comp. Arithmetic, pp.2-8, June 1985.
7. D. Harris, R. F. Sproull, I. E. Sutherland, “Logical Effort: Designing Fast CMOS Circuits”, M. Kaufmann, 1999.