Low – Power Aspects of Different Adder Topologies

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Abstract *– This paper explores different adder topologies for low power solutions. Further, we look at the energy optimization of circuits using transistor sizing technique based on Logical Effort. The efficiency of the method is verified on representative 16-bit adders, commonly found blocks in general purpose DSP processors. The results are shown and analyzed in the Energy-Delay space.*

I. INTRODUCTION

Low power designs are gaining importance in implementations for traditional and emerging portable DSP applications. Recent designs demand increased throughput with low power. The core of DSP integrated circuits has been based on comparisons of gate count and delay based optimization [1]. The focus of this paper is to analyze designs for low power and to understand the tradeoffs in Energy-Delay space.

Adders are important components of all arithmetic units in digital domain circuits. Our analysis includes traditional low-power adder designs for varying performance and Kogge-Stone parallel prefix design in order to explore the extremes of the Energy-Delay space.

II. ADDER DESIGNS

In VLSI design, different adder topologies were proposed. Performance and energy consumption criteria are investigated in order to exploit the benefits of each. Small number of gates allows for significant energy savings. Therefore, at the beginning of our analysis for low power applications we are referring to Ripple Carry Adder structure.

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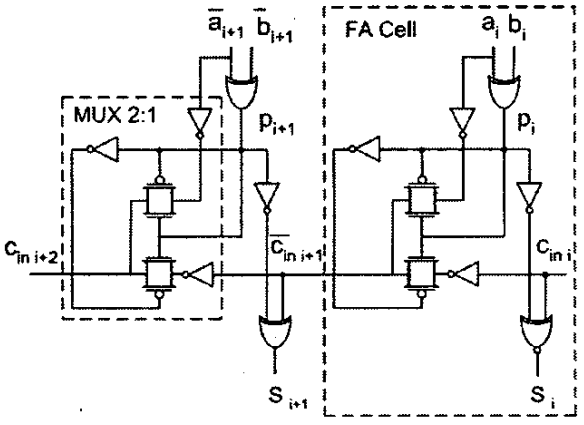

Fig. 1. Full-Adder Cells

The Full-Adder complementary cells used in our implementations are shown in Fig. 1. Multiplexer and XOR cells are implemented with pass-transistor logic gates. To avoid serial connections of pass-gates and ensure signal integrity, we use CMOS inverters. The delay is limited by carry signal which ripples through the cascaded Full-Adder cells and is linearly proportional to the number of bits. As opposed to the speed degradation, Ripple Carry Adder leads to low power due to its small number of transistors.

Other adder structures use multiple gates for propagate and generate signals to reduce the carry path, thus resulting in better delay performance.

In order to keep the power requirements low and close to the cost of ripple carry adder, the next scheme of interest is Carry Skip Adder, CSA [2].

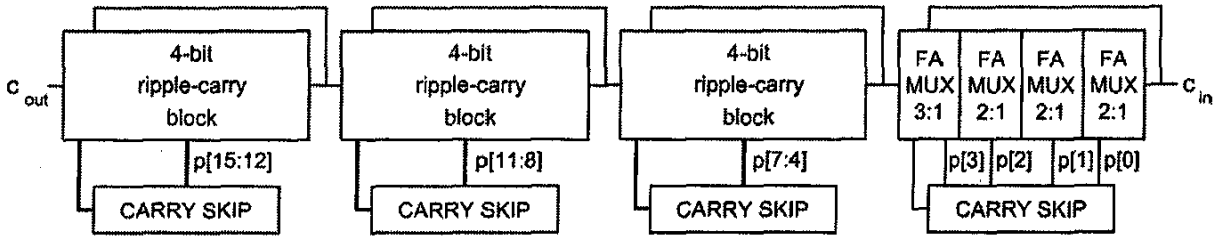

Fig. 2. Block Diagram of Carry Skip Adder

Block diagram of Carry Skip Adder is illustrated in Fig.2. Additional logic required for carry distribution is not excessive and, hence, doesn't impose a big impact in energy consumption. Delay is significantly improved, comparing to the previous ripple carry critical path.

Carry Skip configuration blocks consist of the same elements as the Ripple Carry Adder, instead of the last multiplexer gate in the carry skip path. It is realized as 3:1 multiplexer to select either the locally generated carry signal, propagation of the ripple path from the previous bit or carry skip signal of the group.

Variable Block Adder, VBA, with optimal blocks division yields even better delay performance. Depending on the time required for the carry signal to skip the group of bits, T, optimal division is determined using algorithm described in [3]. The critical path of carry propagation still consists of cascading 2:1 and 3:1 multiplexers, but is sped up comparing to the previously analyzed carry skip scheme.

Fig. 3. depicts the implementation of the carry skip block for the group of five bits used in the analysis of VBA adders.

When high performance is a major issue, tree adder topology is preferred. Unlike CSK and VBA, which rely on modified ripple carry structure to shorten carry propagation path, parallel prefix adders form blocks to pre-calculate the carry signals. Thereby, overall evaluation time is of complexity *O(log n)*.

Graph representation of addition in Kogge-Stone, KS, radix-2 adder implementation [4] is illustrated in Fig. 4. Generate and propagate terms, (1) and (2), are combined into intermediate stages to produce carry signals. The last stage computes sum bits.

Parallel prefix class of adders has minimal logic depth and bounded fan-out at the cost of increased number of carry blocks and interconnections. Allowing logical depth to increase in exchange for fan-out reduction, [5], energy-delay trade-offs are exploited but still the overhead in energy is big comparing to the adder structures analyzed before.

$$g_{i,k} = g_{j,k} + g_{t,j-1} \cdot p_{j,k} \qquad (1)$$

$$p_{i,k} = p_{i,j-1} \cdot p_{j,k}, i < j < k \qquad (2)$$

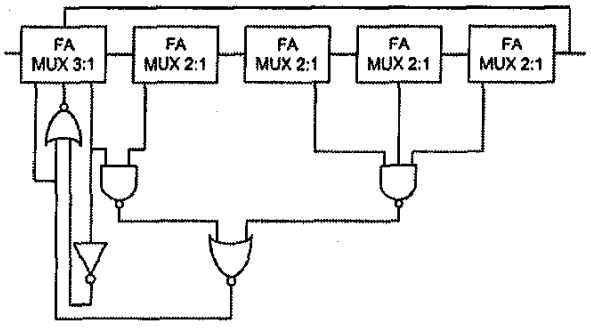

Fig. 3. 5-bit VBA carry-skip block

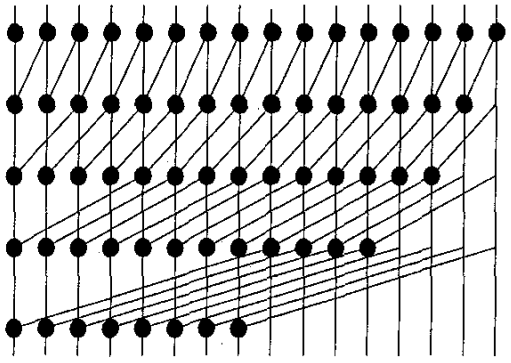

Fig. 4. 16-bit Kogge Stone radix-2 adder

III. ENERGY – DELAY ESTIMATION

A number of techniques for energy-delay modeling and estimation have been studied in literature.
The method of Logical Effort [6, 7] is used as simple and effective method for analysis of delay, while an energy model accounts for gate capacitance as well as parasitic capacitance for energy estimation. These methods are used for comparison of different adders in the energy-delay space [8, 9, 10].

Delay in the Logical Effort model, (3), is expressed in terms of unit delay, τ, of an inverter driving the copy of itself with no parasitics. Driving capabilities and dependencies of the gate delay on input and output load are represented with logical and electrical effort parameters, g and h, respectively. They contribute to the first component of gate delay called stage effort, f. The second component, p, introduces intrinsic parasitic delay.

$$T_d = (gh + p)\tau \qquad f = gh \tag{3}$$

Logical Effort method allows for fast optimization of path delay. Optimal delay is achieved if equal stage efforts are applied in sizing of the gates.

Recent research [9, 10] has shown that redistribution of the gate delays among stages, (4), results in energy savings with no delay expense.

$$f_i = f(1 + x_i) \neq f \ , x_i \in (-1, n) \tag{4}$$

Initial sizing is calculated using equal stage efforts. Under the condition for equal delay, (5), new gate sizing is optimized for the minimum energy.

$$\sum_{i=0}^{n} x_i = 0 \tag{5}$$

The Optimization function, (6), assumes a switching factor, β, equal to one and minimizes the total energy expressed in terms of the sum of the gate widths:

$$S_w = \sum_{i=0}^{n} \frac{\beta W_i}{\prod_{j=1}^{n} (1 + x_j)} \tag{6}$$

Numerically solved equations of LaGrange minimization method for function (6) under constrain for equal delay, (5), provide new sizing, (7).

$$W_{i,x} = \frac{W_i}{\prod_{j=1}^{N} (1 + x_j)} \tag{7}$$

The result of logical effort delay based optimization was to keep the stage efforts constant and maintain the optimal delay. Adopting this new methodology, energy savings are achieved with no cost in delay.

Following section describes the results of new methodology in comparative analysis of different adder topologies for low power designs.

IV. RESULTS

Fujitsu's 0.11μm, 1.2 V CMOS technology is used for the characterization of the gates.

Adders are compared in Energy-Delay space, Fig. 5. The objective is to investigate the tradeoffs.

Two approaches are considered. For a given delay, which adder is the best to use for achieving good energy savings, and, under the energy constraint, different topologies are considered to obtain the best delay performance.

Kogge-Stone adder is analyzed as representative of the class of high performance adders in the lower bound of delay space and to compare with other structures in terms of energy.

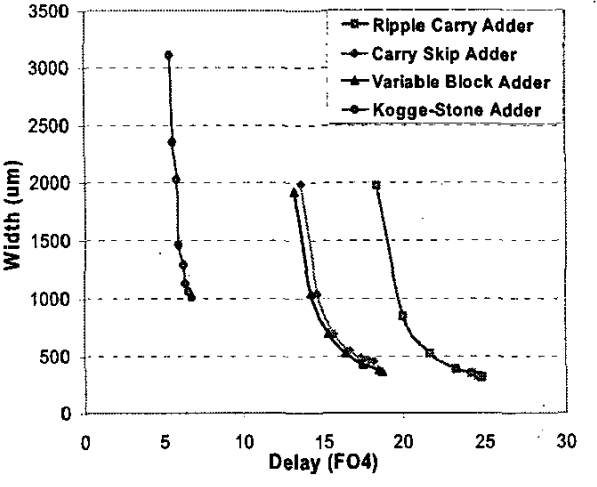

Fig. 5. Adders in energy-delay space

Ripple Carry Adder, Carry Skip and Variable Block Adder are energy efficient. Results imply significant delay improvements in carry-skip and VBA structures, at low energy increase.

In the region below 2000 of equivalent gate width, VBA adder achieves 13 FO4 delay, versus 18 FO4 delay needed for slower RCA. Carry skip adder doesn't provide energy savings, but is slower. We can see that the highest performance is obtained using VBA adder with no energy overhead.

For applications with high throughput demands, using high performance adders will result in minimal delay, but energy consumption increased. As long as frequency operation limit is met, we may defer to using simpler adder structures and trade performance for good energy savings. For applications up to 17 FO4 delay, Variable Block Adder provides the best Energy-Delay curve among other adder topologies. It is shown that Ripple Carry Adder doesn't provide improvements in lowering energy, only runs slower.

V CONCLUSION

Architectural choices of adders are discussed and the potential for energy savings using different adder topologies is demonstrated. Analysis has shown that Carry Skip structures have significant delay improvement with no energy increase compared to Ripple Carry Adder, traditionally believed to gain the lowest energy. Energy optimization method provides circuit sizing at the point of minimal energy and best performance.

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