CONDITIONAL TECHNIQUES FOR LOW POWER CONSUMPTION FLIP-FLOPS

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ABSTRACT: Conditional capture and conditional precharge techniques for high-performance flip-flops are reviewed in terms of power and delay. It is found that application of conditional techniques can improve Energy-Delay Product for up to 14% for 50% input activity and save more than 50% in power consumption for quiet input. This property makes conditional methods suitable for high-performance VLSI systems.

1. INTRODUCTION

Power consumption in high-performance integrated circuits has been one of the most critical constraints in high-performance designs recently. The inefficient cooling technology, increased leakage current with dimension scaling and increased number of transistors on the chip all contribute to the increase in power dissipation in today's VLSI circuits. Power consumption break-ups reported recently show considerably high portion related to the clock generation, distribution and state elements clock consumption: 30-40%. This ratio is expected to grow further due to the constant frequency increase trends and reduction of number of logic gates per pipeline stage. Considerable power savings can therefore be expected from low-power oriented clock subsystem design.

Recently, flip-flop techniques with internal activity gated upon the actual need to carry out signal transition, based on clock pulse generation were introduced [1,2]. The output of the flip-flop is monitored and internal transitions allowed only if it would be used to change the value of the output.

2. CONDITIONAL CAPTURE TECHNIQUE

Conditional Capture technique is presented in [1]. By disabling redundant internal transitions, this technique achieves significant power reduction at little or no delay penalties. Due to this property, it is particularly attractive from the point of view of high-performance VLSI implementations.

Motivation behind Conditional Capture technique is the observation that considerable portion of power is consumed for driving internal nodes even when the value of the output is not changed (corresponding to low input activities). It is possible to disable internal transitions when it is detected that they will have no effect on output.

In [1] two implementations of Conditional Capture technique: single-ended and differential were proposed. Single-ended implementation is more difficult - due to the single-ended nature of the flip-flop (only D=1 state is sampled), disabling the internal transition needs to be accompanied by another mechanism to prevent resetting of the flip-flop when the first stage remains quiet as a result of conditional feature. Thus, an application of locking mechanism that would make a distinction between the sampled zero at the input (D=0) and the case D=1, Q=1 (when the conditional-capture-based flip-flops have different behavior compared to unconditional ones) is necessary in order to preserve FF functionality.

In the proposed implementation (Fig. 1), this is done by direct sampling of (inverted) input in transparency window in single-ended CCFF.

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However, this approach is associated with severe drawbacks, most important of which is related to increased set-up time for sampling zero (low level). This can be concluded from Fig. 1: in order to capture logical '*zero*', D must arrive one inverter delay prior to transparency window (so that transistor stack Mn4, Mn5, Mn6 is on); when capturing '*one*', D should arrive exactly in the transparency window (transistors Mn1, Mn2, Mn3). In other words, there is a systematic mismatch between high-to-low and low-to-high set-up times, which degrades overall flip-flop timing.

Another drawback of CCFF is revealed if a heavier load is presented to the Q output of the flip-flop. Since the high-to-low transition of the output is allowed only in the transparency window, the arrival of D input needs to be set well before it in order to ensure proper discharge of Q before the window is closed. This effect accumulates with the one described above, making the set-up time in high-to-low case limiting performance parameter for this implementation.

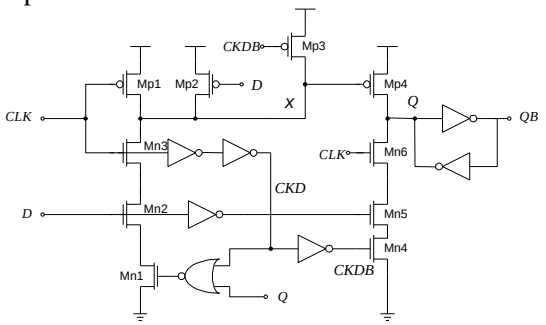

Fig. 1. Conditional Capture Flip-Flop

3. CONDITIONAL PRECHARGE TECHNIQUE

Conditional Precharge technique [2] is another way to save the unnecessary portion of the power in the flip-flop. Instead of gating data capture (evaluation), it is internal node precharge that is conditioned by the state of the output. Conditional Precharge Flip-Flop (CPFF) is shown in Fig. 2a.

With the assumption that the internal node X is precharged (high) when the clock is in the 'low' state, the evaluation of X happens in the transparency window. If the input D is 'high', X goes to the low level, which is used to set the output Q to 'high'. Node X remains low as long as both input D and output Q are at the high level. This allows savings in the power consumed on unnecessary consecutive evaluations and precharges for D=1. High-to-low transition of the output is achieved by sampling high level on X in the transparency window. Also, conditional keeping function is applied at the output to avoid contention with the output keeper - the output is kept low as long as X is high and, similarly, it is kept high outside of the transparency window.

Like CCFF, this flip-flop has the problem of effectively higher set-up time for high-to-low transition due to the requirement to discharge the output before the transparency window is closed. This problem is alleviated by the introduction of small inverter (Inv4b) for controlling the keeper transistor (Mn8), rather than waiting for heavy-load output Qb to make a low-to-high transition.

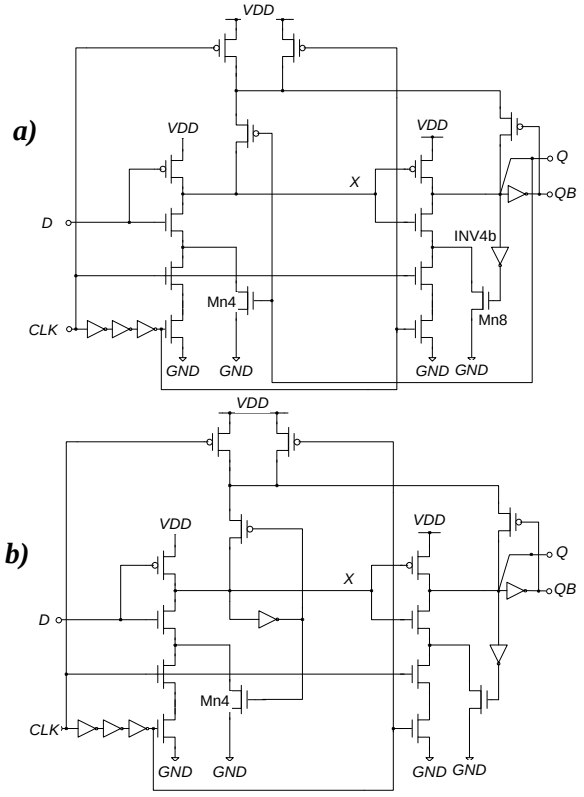

Fig. 2. a) Conditional Precharge Flip-Flop – CPFF, b) Alternative version - ACPFF

This method has two power-related drawbacks. One is the introduction of another critical path (high-to-low case), which increases the size of the p-MOS transistor in the first stage and n-MOS transistors in the second stage. Another problem is the transparency of the first stage of the flip-flop to

the input glitches when the output is at the high level (Mn4 is on when Q=1). This drawback is alleviated by a local inverter connected to the gate of Mn4, as shown in Fig. 2b. This modification inhibits the glitch propagation by employing local, rather than global feedback. Thus, node X cannot make falling transition until the next transparency window.

4. NEW IMPLEMENTATION OF CONDITIONAL CAPTURE TECHNIQUE

Proposed implementation of Conditional Capture feature (Fig. 3) attempts to supply the information on the state of D to the second stage so that excessive low-to-high set-up time is avoided. It uses the first stage transistor stack to sample the input D for the high-to-low transition. The heavier load signal (X) is enabled to evaluate in the transparency window if the output Q is at the low level (so that the evaluation of X makes sense), while another signal, taken directly from the stack (Y) is used to enable or disable high-to-low transition at the output. Unlike signal X, Y carries the information on the state of the input even if the output is at the high level. Due to the lighter load on this node, this evaluation is performed with less power consumption as well.

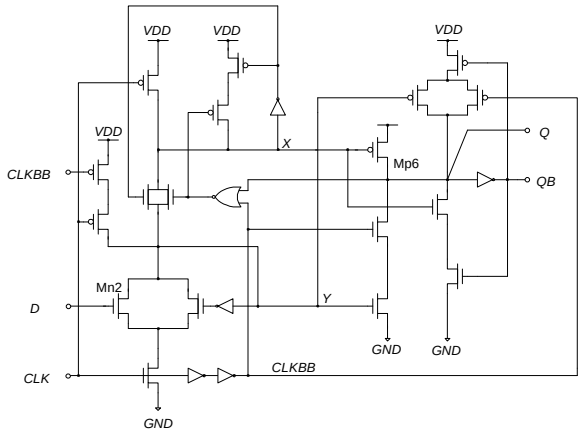

Fig. 3. Improved Conditional Capture Flip-Flop

If the internal node X is evaluated to zero, the output is set to high level by transistor Mp6. The high level on node Y after the rising edge of the clock indicates that D=0, and it is therefore used to reset the output (if it is not already at the low level). Second stage transition to 'zero' is gated by delayed clock to prevent the glitch at the output Q due to the short time needed to evaluate Y.

Both internal signals as well as the output are kept in high and low states by non-conflicting transistors to avoid additional power consumption when evaluating path is overpowering the keepers.

Another good property of this realization is low clock and data load, as well as possibility of logic embedding (n-MOS network instead of single D transistor Mn2).

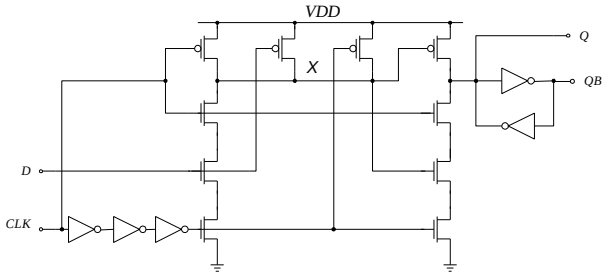

Fig. 4. Hybrid Latch Flip-Flop - HLFF

5. SIMULATION

The simulations are performed with 0.18um Fujitsu transistor models, power supply of 1.8V and nominal temperature of 27°C. Clock frequency was 500MHz. Testbench used for simulation is given in Fig. 5. Energy-Delay Product (EDP) was used as a figure of merit. EDP is obtained as a product of average flip-flop power consumption with 50% data activity [3]. Dissipation of driving circuits for both clock and data are taken into account when calculating power consumption. This way, the effect of the load the circuit imposes to the driving logic is enclosed and influences the total performance.

6. RESULTS

The flip-flops chosen for comparison are CCFF [1], CPFF (we performed a set of simulations to confirm that it also represents ACPFF since they match within 2%), proposed conditional capture-based flip-flop (imCCFF) and non-conditional pulse-latched Hybrid Latch Flip-Flop (HLFF – Fig. 4, [4]). Fig. 6 shows power consumption break-up for activities of 50% and 0% (D=1). It can be seen from the Fig. 6 that savings in internal power vary from 20-30% for activity of 50%, to 50-70% when D input is at the constant high level.

Fig. 7 shows the total power consumption versus input activity. Lower activities at the input result in higher power savings of conditional flip-flops over non-conditional realization, which is what is expected from the internal signals behavior of the flip-flop.

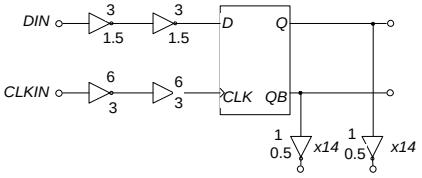

Fig. 5. Simulation Testbench

Table 1 presents overall comparison between the flip-flops. It can be seen that the delay of the devices is somewhat degraded. However, this is not a fundamental constraint of conditional techniques, but only an optimal point in device sizing in terms of chosen optimization parameter - EDP.

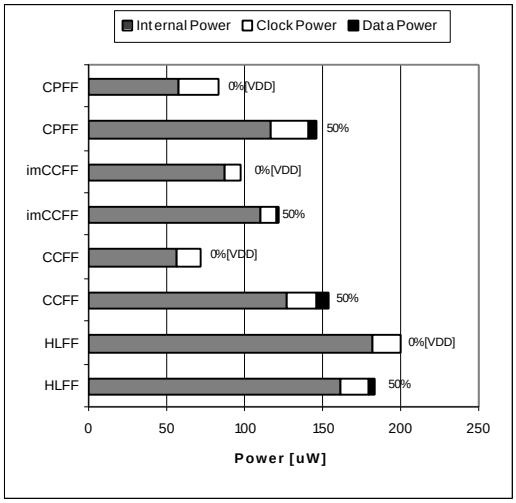

Fig. 6. Power Consumption vs. Data Activity

EDP comparison for activity of 50% shows about 14% and 10% improvement over non-conditional circuit for CPFF and improved CCFF, respectively. It is worth to notice that CCFF from [1] exhibits worse performance even than non-conditional HLFF. This is explained by poor delay characteristic, caused by the failure to reduce flip-flop delay by taking advantage of the negative set-up time.

Table 1. Simulation Results

a = 50%	t_D [ps]	P_{tot} [uW]	P_i [uW]	P_{clk} [uW]	P_D [uW]	EDP $x10^{-23}$ [Js]
CCFF	246.8	153.4	127.3	18.5	7.7	7.6
CPFF	202.3	146.3	117.0	24.4	4.9	5.9
ACPFF	204.1	147.6	118.3	23.7	4.9	6.0
HLFF	187.9	183.8	161.3	18.0	4.4	6.9
imCCFF	257.4	121.7	110.8	10.2	0.7	6.3

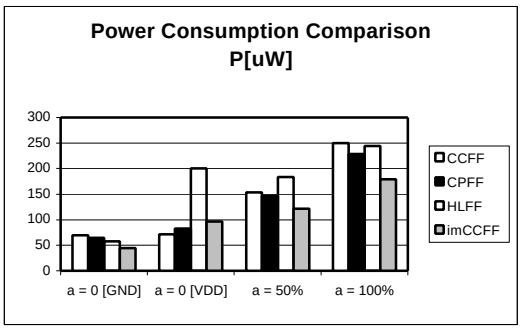

Fig. 7. Power Consumption Comparison

7. CONCLUSION

Conditional internal activity flip-flop techniques are reviewed and their performance evaluated against similar non-conditional methods. It is found that overall Energy-Delay Product can be reduced by up to 14% in the conditions of 50% data activity, while total power saving is more than 50% with quiet inputs.

It can be concluded that state elements equipped with conditional features have advantageous properties, particularly in low data activity conditions. However, as seen on the example of CCFF, circuit implementation solutions play significant role in overall performance.

Consequently, conditional techniques are suitable for the application in the high-performance VLSI circuits in the future.

8. REFERENCES

[1] B. S. Kong, S. S. Kim, Y. H. Jun, "Conditional Capture Flip-Flop Technique for Statistical Power Reduction", Digest of Technical Papers, p290-291, February 2000

[2] N. Nedovic, V. G. Oklobdzija, “Hybrid latch flip-flop with improved power efficiency”, Proceedings of SBCCI, p211-215, September 2000

[3] V. Stojanovic, V. G. Oklobdzija, “Comparative Analysis of Master-Slave Latches and Flip-Flops for High-Performance and Low-Power Systems ", IEEE Journal of Solid-State Circuits, Vol.34, No.4, pp.536-548, April 1999.

[4] H. Partovi, et. al., "Flow-Through Latch and Edge-Triggered Flip-Flop Hybrid Elements," ISSCC Digest of Technical Papers, pp. 132-139, February 1996.